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Test Challenges Faced with System in Package

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Agenda

1. System in Package (SiP) – Introduction
2. Testing SiP Devices
3. Case Study: Testing – 5G SiP Radio Module
Section 1

SIP – INTRODUCTION
What is a System in Package (SiP)?

- Characterized by any combination of
  - One or more ICs of different functionality
  - May include passive components and/or MEMS sensors
  - Spans multiple test expertise domains
    - Hardware
      - Analog/Mixed Signal, Digital, RF
    - Software
      - Firmware, Register Control, Device Drivers
- Assembled into a single package that performs as a system or sub-system
SiP/ SoaB Package Examples

- CASiP – RFPA
- FCSiP – Cellular Tx
- CASiP – RFPA
- CuP FCSiP – RFPA
- FCSiP – RFPA
- FCSiP – WLAN Radio
- FCSiP – WLAN BB
- Hybrid SiP – GPS Radio
- Hybrid SiP – Digital TV
- Fingerprint Sensor
- CASiP – MEMs Microphone
- SMT SiP – 3G Modem
- SMT SiP – Cellular Radio

SoaB = System on a Board

Test Challenges Faced with Systems in Package
SiP/SoaB Reality

• OSATs have the advantage of advanced assembly tools. By leveraging heterogenous integration they create the best systems in package

• OSATs have an extensive range of low cost test capabilities that can be applied to provide competitive solutions

• The few large, vertically integrated companies have an early advantage in terms of system design, architecture and DFT
Product Design/Perfect World

- SiP ready EDA design & manufacturing tools
- Extensive DfT
  - Die level, die-to-die and across system
- Redundancy, self repair and reconfiguration
- Easy physical test access
- Until then – let’s look at
  - Existing test technologies
  - Test strategies
  - Industry gaps
Design for Test

• Cannot be an afterthought – too late then
• Many SiP(s) are a collection of ICs without overall DfT
• Use a blend of individual chip test patterns, functional & system level test. Requires BIST structures
• Other practical physical design aids – allow/plan for
  – Test structures, test pads and sacrificial pads
  – Reduced pin count (RPC) test modes – for probe and strip test
  – Keep out zones for contacting
Section 2

TESTING SIP/SOAB
What could possibly go wrong?

- Thermal Interface Material Degradation
- Dielectric Delamination
- Micro bump Fatigue & Electro-migration
- Underfill Delamination
- TSV Void, Fatigue, & Electro-migration
- BGA Fatigue
- Substrate Trace Crack
- Package Warpage
- Bump Fatigue & Electromigration

Electrical Failures
Forming a Test Strategy

- Time to market?
- Data sheet will be guaranteed by:
  - Design or characterization or production test
- Permissible defect level?
- Budgeted cost of test?
- Needs over product lifecycle?
- What actions will result from the testing?
Test Strategies - Distributed Test Flows

Wafer Probe Test

Cost & Quality

Package Final Test

System Level Test

Probe card technology
Advanced probers
RF probe/KGD/KTD

Full Test Development

Contacting technology
Advanced handlers
Strip test
System Level Test

Copper Pillars
Through Silicon Vias
Thin Wafers & Fine Pitch

WLFO & Embedded Die

WLCSP

SoaB

PoP

Conformal Shield

TMV PoP structure
Multiple Test Insertion Points

- Vital to have distributed test flows
  - Fast feedback
  - Scrap avoidance
  - Protects the customer
  - Over test, over characterize early on
  - Phase out tests as DPPM levels drop
Key Points of SiP Test

• Use appropriate, cost effective tester for the type of ICs
• RF probe – when needed, technology is mature
• Testing myriad power management schemes
• Early over-testing
• Are the ICs mature and well characterized?
• Correlation to end product/application
• Final test trending to system level/one box test
• Cost! Cost!! Cost !!!
SiP w/TSV, SoaB Test considerations

• Check every single TSV?
  – Impractical but a risk area
  – Understand failure modes & mechanisms
  – Sample & use variable test patterns within a lot

• Surface mount devices: PCOLA & SOQ
  – Presence, correct value, orientation, live, alignment,
  – Joints: Short, open, quality

• Understand the physics & causes of failure

• Need not use big iron ATE at all steps
Contacting & Handling Considerations

• Final test hardware
  – Precise electrical contacting, thermal management
  – Gentle handling that doesn’t induce damage
  – High volume sockets: long lifetimes, easily performed cleans & maintenance

• Smaller pad/bump sizes, tighter pitch
  – 22 µm bump, 45 µm pitch
  – At speed WS
  – Sub-zero testing
SiP/ SoaB Distributed Test Flow

1. **Known Good Substrate**
2. **Die/Pkg Attach to Substrate**
3. **Known Good Die/Pkg**
4. **Passives**
5. **Partially Assembled Test**
6. **Assembly Complete?**
7. **YES**
8. **NO**
9. **Wafer Probe/Final Test**
10. **Finished Goods**
11. **System Level Test**
12. **Test Challenges Faced with Systems in Package**
Final Test Considerations

• Apply right combination of tests
  – Functional
    • Map system level tests into ATE patterns
    • Avoid complex “tester on load board” hardware
  – Parametric
  – System level
    • If ICs in the SiP have already been ATE tested ($$$)
    • Don’t spend more ($$$) on ATE test if system level test ($) can work
Actions to take after Test?

• Re-work – very unlikely
• Scrap avoidance – yes with PAT
• Huge opportunities for adaptive test
  – On the fly test program adaptation
  – Feed forward data – downstream decisions
  – Feed back data – correlate/improve earlier tests, designs
• 2D barcode and traceability
  – Link test, bill of materials, machine/manufacturing data
Low Cost System Level Test

- System level test need not be manual load / x1
- One can take advantage of pick and place handlers
- SiP automated system level tester placed under a pick and place robotic handler: M-WeST
- Four 802.11 OBT integrated with handler & Station controller
SiP Test Challenges

Assembly (and passives)
- Surface mount defects that elude inspection
- In-circuit/in-situ test Re-work is not feasible
- Handling partially assembled units
- Heat sink not present
- Thermal control
- ESD concerns
- Depth of outgoing o/s test

Final Test
- Conducted RF test may miss certain failure modes only seen in radiated
- Checking shielding
- Burn-in (the IC(s) Or the module)
- Testing unlidded devices
- Early over characterization
- Correlation to what
- Avoiding costly big iron ATE test

Wafer Probe
- Cycles of learning – more probe coverage
- No solutions for dual sided signal probe
- KGD shift during subsequent processing
- Some pitches too fine to probe
- Structures may lack I/O &/or ESD protection
- Multi z level stacks (CoW)

Test Plan - DFT/DFM
- Permissible defect level
- Maturity of the IC(s)
- What to CZ Versus 100% test
- Ability to simulate system
- Cooperation across IDM IC suppliers
- Any self test or self repair
- Electrical accessibility
- Dependence on functional test
- Structural tests
- Balance between SLT vs ATE test
- Substitutability of critical passives
- Traceability requirements
- IoT SiP with sensors/actuators
SiP Test State of the Art & Approaches

Assembly (and passives)
- Use in-situ distributed test flow at key points for scrap avoidance (don’t add more value to the module if already defective)
- Use handler active thermal control as needed if the heat sink(s) are not present yet
- Analysis of what belongs in outgoing o/s test versus what belongs in final test

Final Test
- Unlidded devices – involve socket & handler makers
- Continuous feedback to assembly and probe
- Adaptive test & feed forward, feed back
- Avoiding costly big iron ATE test
- SLT – start LVM on standard handlers, can map a path to semi-custom massively parallel SLT handlers

Wafer Probe
- Dual height (2 level) probe cards available for CoW
- Pick the appropriate ATE tester (RF, MS, memory)
- Aim for KGD, beyond KTD
- Use of RF probe, use of direct dock
- Move cold test from FT to probe
- Get feedback from final test and continually improve probe coverage
- Leverage adaptive test & feed forward, feed back

Test Plan - DFT/DFM
- Plan for early over characterization
- Extra room – add test access!
- Do a test FMEA of the BoM
- Cost model the SLT vs. ATE tradeoffs
- CZ & Qual multiple suppliers of critical passives
- Leverage 2D codes for traceability
- Stimulus test for IoT with sensors/actuators

Test Challenges Faced with Systems in Package
## SiP Test – by Module Type

<table>
<thead>
<tr>
<th>Module Type</th>
<th>Wafer Probe for SiP</th>
<th>PAT</th>
<th>SiP Final Test ATE</th>
<th>SiP Final Test SLT</th>
</tr>
</thead>
<tbody>
<tr>
<td>Radio (PA, Xcvr, FEM, FES)</td>
<td>ATE RF KGD direct dock</td>
<td>Sub-Modules</td>
<td>Custom or Commercial Rack n Stack</td>
<td>Have seen sampling before using R&amp;S or Agilent base station emulator</td>
</tr>
<tr>
<td>Sensory (Biometric, Si microphones)</td>
<td>Typically at IDM fab</td>
<td>Uncommon</td>
<td>Stimulus + Simple ATE</td>
<td>Custom by application/customer</td>
</tr>
<tr>
<td>Companion (WLAN, WiMax, GPS, TV)</td>
<td>RF ATE</td>
<td>Uncommon for simple modules</td>
<td>Skipped</td>
<td>One box testers</td>
</tr>
<tr>
<td>Automotive (Infotainment, ECU, Sensors/Actuators)</td>
<td>Cold probe to avoid tri temp final test</td>
<td>Some frequency for scrap avoidance</td>
<td>Most complex modules get no ATE final test</td>
<td>Customer board</td>
</tr>
<tr>
<td>Baseband (Digital, Memory, PMU, Audio, Digital+RFA)</td>
<td>Cold probe, direct dock Two level probe card (CoCoW)</td>
<td>More common – hdgh end GPU - for scrap avoidance. ATC</td>
<td>MS/SoC PMU Memory</td>
<td>Asynchronous handlers</td>
</tr>
</tbody>
</table>

Test Challenges Faced with Systems in Package
Section 3

CASE STUDY – TESTING 5G SIP RADIO
mmWave Test Coverage Summary

- **Sub 6 GHz**
  - CW Testing (no risk)
  - Modulation (< 64 QAM)
  - Carrier Aggregation (< 80 MHz)

- **mmWave ( > 28 GHz < 80 GHz)**
  - Contacting (available solutions)
  - Test instruments (need to acquire)
  - Calibration Standards for production
  - Wide Bandwidth CA (800 MHz)
Testing 5G Hypothetical Radio Module

- All individual components are tested before assembly
- Antenna assembly is built and tested before die/package attach
- Partially Assembled Test (PAT) of the module is performed as system is being built

Partially Assembled Test (PAT)

Stage 1: Antennas Mounted on back side of substrate (Known Good Package)

Stage 2: Shared Components

Stage 3: Add Rx Module

Stage 4: Add Tx Module

ATE Based Parametric Test

SLT Based Functional Test

Test Challenges Faced with Systems in Package
System Level Test

System Level Tester
(One Box Tester or Rack & Stack)

- Country/Carrier Specific Compliance Testing
- Protocol Testing
- Standard Specific Conformance Testing
- Functional Testing

Command & Control

Test Challenges Faced with Systems in Package
Conclusion

- From the outside System Level Test gives the impression that is built up of the same set of pieces. However, system level testing for SiP or SoaB products require solutions that are as unique as the product line.