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Fan Out Technology Overview

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National Centre for Advanced Packaging (NCAP China)

BiTS China Workshop
Shanghai
September 7, 2017
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- Fan out Technology Introduction
  - Market analysis
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  - Main process technologies
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- Consortium Updated
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NCAP Overview

- Established in Wuxi in 2012
- 10 investors
  - Including the Institute of Microelectronics and the largest OSATs and substrate companies in China (JCAP, NT Fujitsu, WLCSP, ANJILI, WULIWANG, SCC, NDB, IME, Hua Tian, XIN Sheng Kuai Jie)
- Independent business entity
NCAP Platform

Wuxi Headquarters
- 3000m² Cleanroom
- Class 10/100/1,000/10,000
- 8”/12” wafer

Beijing Center
- 1000m² Cleanroom
- Class 1,000/10,000

• R&D & Engineering with 9000m²
• Engineering assembly & metrology equipment with ¥160 million, fixed total equipment value ¥345 million.
R&D Infrastructures

address: Building D1, China Sensor Network, International Innovation Park, 200 Linghu Boulevard, WuXi, Jiangsu Province, China
Industry / Institute Collaboration

- collaborate with industry partners and institutes, proceed small quantity of manufacturing
Why Fan-out

Performance
- Shorter interconnect length, high speed application;
- Superior package level reliability;
- Excellent board level reliability

Cost Advantage
- Substrate /gold free,
- Scalable to the large panel (600mm above)

Form Factor
- Thinner package,
- Package size Scalability

I/O density
- Small pitch,
- High pin counts
Fan Out Market Forecast

Fan-out activity forecast (300mm eq wafers) breakdown per end-market

- 1M+ wafers in 2017
- 4.5M in 2021

Apple's example will show competitors the way

Executive Summary
Fan Out Applications

FAN-OUT APPLICATIONS
Where do we find fan-out? Some examples below

Orange: devices found in FOWLP packages today
Green: future devices that could be found in FOWLP
Grey: devices that will likely remain on WLCSP or flip-chip package, or move to 3DIC or embedded die

Apple iPhone 7 (2016)
A10 APE – InFO package (TSMC)

Samsung Galaxy S7 (2016)
Qualcomm Audio Codec
WCD9335 – eWLB package (Nanium/STATSPack)

Power Management
Marvell
PM920

Spreadtrum
SC2712A

Intel-Mobile/Infineon
PMB5712, PMB5726

Baseband
Spreadtrum
SC8502

Intel-Mobile/Infineon
PMB9600, PMB9810, PMB9801

RF
Spreadtrum
SC8502

Bosch MRR1Plus Radar (2015)
Inferen RASIC™ (77GHz RADAR System IC Chipset) – eWLB package
Continental ARS400 Radar (2015)
NXP MR2001 (77GHz multichannel RADAR) – RCP Package

BK Ultrasound Sonic Window (2015)
Multichip Module – eWLB Package (Nanium)
Keynote: Fan Out Technology Overview

Fan Out Market Development

FAN-OUT ACTIVITY - MARKET FORECAST (1/2)

Fan-out activity revenue forecast ($M)
Breakdown by fan-out market type

- $3,000M: Entry of A10 APE for iPhone 7, 7+, and newer from 2016 - 2016 - 2021 CAGR is estimated at 40%
- $2,500M: After the first jump, further acceptance by players other than Apple (Mediatek? Samsung? Qualcomm?) will occur, maintaining the growth
- $2,000M: Market estimated to exceed $2.5B by 2021
- $1,500M: Intel Mobile/Infineon eWLB-driven
- $1,000M: CAGR > 30%
- $500M: $80M
- $0M

Confirmation phase: Apple keeps its APE in FO and other players follow the trend

Intel Mobile/Infineon eWLB-driven

Transition phase
CAGR ~ 10%

CAGR ~ 80%

CAGR ~ 20%

~$2.5B

The Apple example will show the way to competitors


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Fan Out Market Scale

FAN-OUT ACTIVITY - MARKET FORECAST
Breakdown by product type and evolution

- The "core" fan-out market is evolving:
  - BB/Wireless, PMU/PMIC, and RF are the main driving applications, but fan-out has improved and qualified for MEMS and other non-mainstream products
  - Fan-out is starting to appear in wider applications: GPS modules, Wi-Fi applications, Audio codec, and some specific niche automotive and medical applications
- "HD" fan-out APE/GPU and complex applications will comprise the majority of the fan-out market (high revenue), fueled by iPhone followers
  - Fan-out’s higher integration capability will offer access to markets where flip-chip PoP/SiP currently dominate
  - More complex applications will follow stacked memory, ASICs, CPU/GPU, etc.

Total 2014: $174M
Total 2017: $821M
Total 2021: $2674M
Global Fan Out Market Capacity

FOWLP - ALREADY-INSTALLED CAPACITY

- At the end of 2016, fan-out investments were already very important, and consequently so is capacity
  - With a capacity of 100,000 wafers/month, TSMC’s InFO product has the largest capacity
  - Other main manufacturers are established eWLB providers: Namilum and STATS ChipPAC. Each can produce around 10,000 wafers per week.
  - STATSChipPAC is enlarging its capacity to raise production
  - Since TSMC’s action was quite formidable, investment in equipment for 2017 will not be as high - but it will still be decent:
    - Led by newcomers willing to have a FOWLP offer
    - As well as major players willing to enlarge their capacity (STATSChipPAC and potentially ASE together with Deca)
- With 4.5M wafers to be produced in 2021, capacity must be increased by TSMC and/or other actors. Therefore, a second wave of investment will occur later on; otherwise, capacity be insufficient for addressing the FOWLP market if it keeps growing (see the following slides).

- TSMC has an enormous capacity of 100k wafers per month

- Strong capacity capability already exists with other players too, and it will keep expanding
Development Trend

Performance (L/S; pitch; multiple die, etc.)

Single chip to Multichip, Development from two dimensional to three-dimensional

Cost

APE, FPGA, CPU, GPU, etc.

BB, PMU, RF, GPS, MEMS, etc.
Technology Challenges

Materials
- TBDB (can withstand 260°C)
- Mold material/carrier to achieve low warpage

Equipment
- Die placement (panel level) UPH>10K
- To achieve low cost warpage (TBDB machine: mechanical/thermal/laser)

Process
- Low warpage of package
- Low CTE to achieve high reliability
Major Fan Out Technologies

- **eWLB (wafer level)**
  - First fanout patent filed at 2001
  - Shipped out 1 billion units since mass production in 2009

- **RCP technology**
  - (wafer level), from frees, and licensed NEPES,
  - Low volume shipment

- **TSMC InFO (wafer level)**: Apple used this technology in iPhone 7 (A10 processor).

- **Others (e.g., DECA (chip face up panel level)) technology**: ASE licensed this technology (panel level, and ship out 100 million units).
## Key Player Technology

### FAN-OUT - KEY PLAYERS’ ACTIVITY SUMMARY (1/2)

<table>
<thead>
<tr>
<th>Key Player</th>
<th>Production status</th>
<th>Production information</th>
<th>Technology</th>
<th>L/S minimal features (2016)</th>
<th>Driving applications</th>
<th>Driving customers</th>
</tr>
</thead>
</table>
| **ASE (TW)**   | In volume production on 300mm (e-WLB and in-house fan-out) | - Production on 200mm until 2012  
- 300mm volume production since 2015  
- In 2016, fab start for panel manufacturing (M-series) | e-WLB license (Chip-first face-down)  
M-Series license (Chip-first face-up) | 5um L/S | BB, PMU, RF | Qualcomm, Mediatek |
| **STATS ChipPAC (SG)** | In volume production on 300mm and 330mm | - >10,000 wafers/week  
- >1B units sold since 2009  
- R&D ongoing for production on panels | e-WLB license (Chip-first face-down) | 5um L/S | BB, PMU, RF | Qualcomm, Broadcom, Spreadtrum, Cirrus Logic, Mediatek |
| **Deca Technologies (US)** | In volume production on 300mm  
Line creation for panel ongoing | - >100 million units since 2011  
- Panel production 80% ready | M-Series (Chip-first face-up) | 5um L/S | BB, PMU, RF | Cypress, Qualcomm |
<p>| <strong>NANION (PT)</strong> | In volume production on 300mm | - &gt;500 million units on the market since 2010 | e-WLB license (Chip-first face-down) | 5um L/S | BB, PMU, RF, GPS, MEMS | Qualcomm, Marvell, Mediatek |</p>
<table>
<thead>
<tr>
<th>Key Player Technology</th>
<th>Production status</th>
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<th>Driving applications</th>
<th>Driving customers</th>
</tr>
</thead>
<tbody>
<tr>
<td>SPIL (TW)</td>
<td>R&amp;D and sampling</td>
<td>Production capability since 2015 on 300mm wafers</td>
<td>SLIT (Chip-last with fab BEOL)</td>
<td>&lt;1µm L/S expected</td>
<td>FPGA, CPU, GPU</td>
<td>Xilinx</td>
</tr>
<tr>
<td>Amkor (US)</td>
<td>R&amp;D and sampling</td>
<td>Production capability since 2015 on 300mm wafers</td>
<td>SWIFT (Chip-last), SLIM (Chip-last with fab BEOL)</td>
<td>2µm L/S expected (SWIFT), &lt;1µm L/S expected (SLIM)</td>
<td>BB, PMU, RF, APE, CPU/GPU</td>
<td>?</td>
</tr>
<tr>
<td>TSMC (TW)</td>
<td>In volume production on 300mm</td>
<td>300mm volume production since 2016</td>
<td>InFO (Chip-first face-up)</td>
<td>5µm L/S</td>
<td>APE</td>
<td>Apple</td>
</tr>
<tr>
<td>Nepes (KR)</td>
<td>In volume production on 300mm</td>
<td>300mm volume production since 2013 (previous experience in Singapore since 2009)</td>
<td>RCP license (Chip-first face-Down)</td>
<td>5µm L/S</td>
<td>BB, PMU, RF, APE</td>
<td>NXP, Sony</td>
</tr>
<tr>
<td>PTI (TW)</td>
<td>R&amp;D and line creation</td>
<td>510 x 515mm panels - volume production expected in 2017</td>
<td>CHIEFS (Chip-first), CLIP (Chip-last)</td>
<td>2µm L/S expected</td>
<td>BB, PMU, RF, APE, FFGA, GPU</td>
<td>?</td>
</tr>
</tbody>
</table>
Major IPs for Fan out

RDLs to fan out the circuitry from die edges without using substrate

**United States Patent**

**Inventors:** Harry Hedder, Germering (DE); Thorsten Meyer, Erlangen (DE); Barbara Vasquez, Munich (DE)

**Assignee:** Infineon Technologies AG, Munich (DE)

**Filed:** Oct 31, 2001

**Published:** US 6,727,576 B2

**Date of Patent:** Apr 27, 2004
Global IP Distribution

- 6137 Patents
- 8837 Patent Families

Trend of patent application

Applicant patent date

TAIWAN SEMICONDUCTOR
TSMC
STATS CHIPPAC
INTEL
INFINEON
FAN-OUT TECHNOLOGY
SAMSUNG ELECTRONICS
QUALCOMM
AMKOR TECHNOLOGY

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Infineon’s Embedded Wafer-Level Ball Grid Array (eWLB)

Schematic process flow for a fan-out wafer-level package

Test for KGD
a) Wafer Singulation
b) Reconfigured Wafer
c) Redistribution
d) Ball Apply + Singulation

Molded reconfigured wafer

Fan-Out Area (Mold)
Redistribution Layer (RDL)
Chip
TSMC InFO Main Process

TSMC InFO-WLP
(Integrated Fan-Out WLP)

At the TSMC Technology Symposium in San Jose, CA in April 2014, TSMC announced the latest InFO-WLP platforms:

- 8mm x 8mm is targeted at RF and WiFi chips
- 15mm x 15mm is targeted at application processor and baseband chips
- 25mm x 25mm could be applied to GPU and networking chips
TSMC InFO PoP Structure

**TSMC’s InFO_PoP**

- **Conventional PoP for Application Processor (AP) chipset**
- **TSMC’s PoP for Application Processor (AP) chipset**

<table>
<thead>
<tr>
<th>Orange: devices found in FOWLP packages today</th>
<th>Green: Future devices found in FOWLP packages</th>
</tr>
</thead>
<tbody>
<tr>
<td>Apple iPhone 7 (2016)</td>
<td>Samsung Galaxy S7 (2016)</td>
</tr>
<tr>
<td>AT1APE – InFO package (TSMC)</td>
<td>Qualcomm Audio Codec</td>
</tr>
<tr>
<td>WCD9335 – eWLB package (Nanium/STATS ChipPAC)</td>
<td></td>
</tr>
</tbody>
</table>

Eliminated solder bumps, underfill, and package substrate. Lower Profile!
<table>
<thead>
<tr>
<th>OSAT in China</th>
<th>Packaging Fan out Technologies available</th>
<th>status</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hua Tian Scientific Co., Ltd</td>
<td>eSIFO ™</td>
<td>Qualified and engineering samples are ready; and ready for ramping in the production</td>
</tr>
<tr>
<td>JCET</td>
<td>MIS technology based</td>
<td>Ready for mass production</td>
</tr>
<tr>
<td>NT Fujitsu</td>
<td>Panel level fan out</td>
<td>In development</td>
</tr>
</tbody>
</table>
NCAP WL Fan out Test Results

Circuit Resistance vs. Circuit Length

Chip Pad1 - Chip Pad27

Chip Pad3 - Chip Pad11

Resistance vs. Chip Pad ID

September 7, 2017
Large Panel Fan Out Consortium

**Objective:** Development and characterization of large panel fan out design, process and reliability, provide supply chain analysis and justification for commercialization.

<table>
<thead>
<tr>
<th>No.</th>
<th>Key members</th>
</tr>
</thead>
<tbody>
<tr>
<td>1</td>
<td>NCAP</td>
</tr>
<tr>
<td>2</td>
<td>SCC (深南)</td>
</tr>
<tr>
<td>3</td>
<td>SPIL (Taiwan)</td>
</tr>
<tr>
<td>4</td>
<td>Sinopaco (中鶴)</td>
</tr>
<tr>
<td>5</td>
<td>AMC (Taiwan)</td>
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<tr>
<td>6</td>
<td>Delphilaser (德龙)</td>
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<td>7</td>
<td>Fujitsu</td>
</tr>
<tr>
<td>8</td>
<td>TOWA</td>
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<tr>
<td>9</td>
<td>Bee-semi(中电科)</td>
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<tr>
<td>10</td>
<td>JSR</td>
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<tr>
<td>11</td>
<td>Screen</td>
</tr>
<tr>
<td>12</td>
<td>KohYoung (高永)</td>
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<tr>
<td>13</td>
<td>Savansys</td>
</tr>
<tr>
<td>14</td>
<td>Huawei</td>
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<tr>
<td>15</td>
<td>Mascem (技美)</td>
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<td>16</td>
<td>Sumitomo</td>
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<tr>
<td>17</td>
<td>Shin-Etsu (信越)</td>
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<tr>
<td>18</td>
<td>DNP (大日本印刷)</td>
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<tr>
<td>19</td>
<td>ASM</td>
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<tr>
<td>20</td>
<td>Ingenic (君正)</td>
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<tr>
<td>21</td>
<td>ORC</td>
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<td>22</td>
<td>SCHOTT</td>
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<tr>
<td>23</td>
<td>Atotech</td>
</tr>
<tr>
<td>24</td>
<td>See ray</td>
</tr>
<tr>
<td>25</td>
<td>Lenovo</td>
</tr>
</tbody>
</table>

Fujitsu, SPIL, SCC

Material/equipment suppliers

NCAP (industry & commercialized Partner)

End users (Huawei, Lenovo)
Consortium Key Members

Membership fee: US$20K
Paying members: 15 companies
Supporting members: 10 companies
Panel Level Fan Out Consortium

Consortium on Low Cost Panel Level Fan-out Technology Development

- 25 International Companies joined the Consortium
- Target single die fan-out (one layer RDL) development & demonstration (Phase 1)
- Establish design, simulation, process capability and panel level fan-out supply chain build up
- Complete single die fan-out lesson learnt and preliminary process & reliability qualification
- Drive low cost solutions & commercialization
- Establish panel level fan-out technology Industry chain embryonic in China
### Die First Process

**Package structure**

<table>
<thead>
<tr>
<th>Die First Process</th>
<th>Lamination</th>
<th>Die Attach</th>
<th>Panel Molding</th>
<th>2nd Bonding</th>
<th>RDL</th>
<th>UBM</th>
<th>Ball Drop</th>
<th>Testing</th>
</tr>
</thead>
</table>

- **Package size**: 8.9 x 7.7 mm
- **RDL**: 1 layer
- **RDL Line/Space**: 20/20μm
- **Ball Pad Size**: 250 μm
- **Ball Pad PI Open**: 230 μm
- **Die sizes**: 5.24 x 4.835mm
- **Die pad pitch**: 96 μm
- **Die thickness**: 200 μm
- **Die Pad PIO**: 65x65 μm
- **Die Pad Qty.**: 207

### Key Benefits

- Have advantage of easier process
- Thinner than flip chip package (no substrate)
- Support increased I/O density
- Excellent electrical and thermal performance
- Excellent high temperature warpage performance
- Fine line & space
- Panel level molding process
- Establishing panel level fan out industrial base
Die Last Process

Package structure

Package size: 8 x 8 mm
Package ball Qty : 185
Substrate Line: 1 layer
Line/Space: 30/30um

Die sizes: 6 x 6 mm
Die pad pitch: 200 μm
Die Thickness: 150 μm
Cu pillar height : 70um
Copper pillar Qty.: 203

Key Benefits

- Utilizes a Low Cost FC Coreless Substrate
- Panel processing (low cost)
- No FO Wafer Fab Investment needed, can use existing Flip Chip Packaging manufacturing lines
- Fan-Out Packages with low thickness
- Design based on flip chip die
- Test as module as usual
- Establishing panel level fan out industrial base
Major Results Sharing

Die First Process

Die Last Process

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Conclusions

1. Fan out technologies are commercialized in the major forms of eWLB, RCP, InFO, and other mixed technologies.

2. The market will be booming for fan out especially after Apple iPhone 7 was using InFO technologies. LPFO will be commercialized soon.

3. The material and equipment suppliers are facing challenge of supplying qualified solutions with time frame and low cost.

4. China will be the hot place to execute fan out manufacturing and products in next 5 years.
Thank You!

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Innovate Incubate Influence Impact

Value
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