TEST TOOLING MADE EASY

Whether you’re testing conventional packages like QFNs and BGAs, or emerging 2.5D and 3D packages, you’re only as successful as your test floor equipment. This session’s presenters span the spectrum of tooling issues beginning with a method for 3D package handling through the integration of complex technologies. Next, you’ll learn how to prevent semiconductor test system coolant leakage by implementing a hazardous warning system. Operator error in manual test handlers comes under scrutiny thanks to a failure analysis investigation in QFN packages. Lastly, we take a look at cost saving through homogenous spring pin tip implementation in a high volume manufacturing (HVM) environment.

3D Package Handling: A Simple Case of Integrating Complex Technologies
Zain Abadin—Advantest America, Inc.

Innovative Way to Prevent Semiconductor Test Tester Coolant Leakage with Hazardous Warning System
Yee Wei Tiang—Intel (Malaysia)

Die-Cracking Failure Analysis of QFN Packages in Manual Test Handler
M.P. Divakar, PhD—Stack Design Automation

Cost Saving Through Homogenous Spring Loaded Pin Tip Implementation in High Volume Manufacturing (HVM) Environment
Chin Siang (David) Chew, Nithya Nandhan Subramaniam—Intel Technology
Chin Chien Tee—Interconnect Devices, Inc.

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3D Package Handling
A Simple Case of Integrating Complex Technologies

Zain Abadin
Advantest America, Inc.

Contents

• Scope and Basic Assumptions
• 3D Package Trends
• 3D Package Handling Technologies
• 2/2.5/3D Package Handler
• Conclusions
Scope and Basic Assumptions

Scope
Final Test
3D packages include 2D, 2.5D, 3D Singulated, SiP/PoP

Basic Assumptions
New handling solutions
- Improve or maintain current yield
- Deliver competitive CoT
- Suitable for HVM environment

Yield Applied

Unit Cost = Depreciation + Operating Cost / Throughput

3D Package Trends
Market Forces

- Higher Performance
- More Features
- Smaller, Thinner
- Lower Cost

Why 3-D?
"More than MOORE"

Driving Forces for 3D Integration

Sources: Micron Technology, EE Times, ITRS 2009 Assembly, Google Images
3D Package Trends

Market Forces

- Higher Performance
- More Features
- Smaller, Thinner
- Lower Cost

Why 3-D?

<table>
<thead>
<tr>
<th></th>
<th>2D</th>
<th>3D</th>
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<tbody>
<tr>
<td>Size Reduction</td>
<td>35%</td>
<td>45%</td>
</tr>
<tr>
<td>Power Consumption</td>
<td>40%</td>
<td>45%</td>
</tr>
<tr>
<td>Packaging Cost</td>
<td>40%</td>
<td>45%</td>
</tr>
</tbody>
</table>

Sources: Micron Technology, EE Times, ITRS 2009 Assembly, Google Images

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3D Package Trends

Industry Examples

Source: Xilinx 3-D_Architecures

Source: Amkor Technologies, Inc

Xilinx Virtex-7

Package Substrate

Microbumps
Silicon Interposer
Through-Silicon Vias
C4 Bumps
BGA Balls

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### 3D Package Trends

**Packaging Trends and Handler Functions**

**Handler’s Main Functions:** Transfer, Align, Thermal Control

- **Loading** + Pre-Soak
- **Transfer**
- **Align** + Thermal Control
- **Transfer** + Post-Soak
- **Unloading**

**Test Site**

**Packaging Trends**
- Finer Ball Pitch
- Heterogeneous Stacked Devices
- High Power Dissipation
- Thinner Packages
- High Pin Count

Source: Daniel Nenni, Semiconductor Packaging (3D IC) Emerging As Innovation Enabler!

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**3D Package Trends**

**Test Nodes**

No industry consensus on test nodes yet

*Niels Bohr*  
“Prediction is very difficult, especially about the future.”

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3D Package Handling Technologies
Packaging Trends and Handler Requirements

**Packaging Trends**
- Finer Ball Pitch
- Power Dissipation
- Heterogeneous Stacked Devices
- Thinner Packages
- High Pin Count

**Handler Requirements**
- Vision Alignment

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3D Package Handling: Alignment
Tolerance Stack Up @ Contact

Major Contributors to Tolerance Stack up @ the Contact
- Socket
- Package
- System Positioning
### 3D Package Handling: Alignment

#### Mechanical Alignment Method

- Pin Diameter
- Pin to Guide
- Pin Position

1. **Guide Outline**
2. **Device**
3. **Error in Alignment**

#### Vision Alignment Method

- Measure socket position and angle
- Calculate and Compensate: x, y, theta
- Measure device position and angle

Result: High fidelity alignment
3D Package Handling: Alignment
Trend towards Vision Alignment

Alignment Simulation

Miscontact Ratio (%) Ball Pitch vs Alignment Method

>33%

Ball Pitch (mm)

Benefits:
- Improved yield
- Lower CoT

3D Package Handling: Thermal
Current Handler Segmentation and Trends

Memory Handler
Chamber, LN2 for low temp

SoC Handler
For Low Power Dissipation: ATC, PTC
For High Power Dissipation: ATC, PTC

Trends:
- Segmentation disappearing
- Higher Power
- Higher Power Density
- Thinning Packages
3D Package Handling: Thermal
ATC Method and Performance

Watch for:
- Thermal Mass
- Temp. Transition
- Tj max/min,
- Time to Guard Band
- Induced Gradient
- SP vs. Power/Power Density
- ATC+PTC in same system

3D Package Handling: Thermal
ATC Performance Examples

Resistance (C/W) at
45 W, 100 W, 130 W, 200 W
**3D Package Handling: Thermal**

**Thermal Trend and ATC Need**

**Power and Power Density**

- **Thermal concerns**
  - E.g. Optical 85°C junctions

Source: Xilinx 3-D_Archiectures

**Power Density > 50 W/cm²**

<table>
<thead>
<tr>
<th>Year</th>
<th>Logic + Memory</th>
<th>Power &gt; 10x</th>
</tr>
</thead>
<tbody>
<tr>
<td>2010</td>
<td>~ 5x</td>
<td></td>
</tr>
<tr>
<td>2012</td>
<td>1x</td>
<td></td>
</tr>
<tr>
<td>2014</td>
<td></td>
<td>~ 5x</td>
</tr>
</tbody>
</table>

**Benefits:**
- Improved yield,
- Lower TT
- Lower CoT, Higher ASP

**3D Package Handling: Thin**

**Impact Force and Force Centroid**

**Impact Force During Transfer**

< 0.3 N

**Force Centroid**

Source: Bernd Appelt: The Thin Package Challenge Never Ends, Semicon West 2012

**Smart Phones < 8 mm**

**Tablets < 10 mm**

**Notebooks < 20 mm**

**Wearable Electronics**
Rapid Increase in Pin Count
Trend towards Higher Parallelism
Translate into Higher Insertion Force, >4000 kg

Collaboration: Lowering F/Pin will be great help
Summary

- 2.5D in production
- Packages becoming more complex, existing advanced technologies capable of handling each handling requirement - separately
- 3D package handling need an integration of ATC/PTC + VA and STH technologies
- Upgradeable solution needed to accommodate future migration to finer pitch, higher parallelism and higher pin count

One correction:

3D Package Handling:
A Complex Case of Integrating Simple Technologies