“Revolutionizing High-Speed Socket Test”
Michael de Bie
Exotest
Boris Coto, Rafiq Hussain
Advanced Micro Devices

“Understanding Impact of Burn-in Sockets on Fragile Semiconductor Packages Using Finite Element Analysis”
Prasanth Ambady, Keith Crowe, Hide Furukawa
Sensata Technologies

“Contact Resistance is Sexy Again”
Tim Swettilen, Morten Jensen
Intel Corporation

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Interconnect Challenges

Faster Devices Need Higher Bandwidth!

- More Pins
- Faster Speeds
- Dedicated
  - Serial IO
  - RapidIO
  - HyperTransport
  - DDR2
  - FBDIMM
  - FibreChannel
  - Gigabit Ethernet
  - SATA/SAS
Got Enough Bandwidth?

<table>
<thead>
<tr>
<th>Standard</th>
<th>Max Data Rate</th>
<th>Bandwidth Required</th>
</tr>
</thead>
<tbody>
<tr>
<td>DDR2-533</td>
<td>1.066Gbps</td>
<td>2.132GHz</td>
</tr>
<tr>
<td>&amp; DDR2-800</td>
<td>1.6Gbps</td>
<td>3.2GHz</td>
</tr>
<tr>
<td>3.0</td>
<td>2.8Gbps</td>
<td>5.6GHz</td>
</tr>
<tr>
<td>2.0</td>
<td>5.2Gbps</td>
<td>10.4GHz</td>
</tr>
<tr>
<td>1.0</td>
<td>3.125Gbps</td>
<td>6.25GHz</td>
</tr>
</tbody>
</table>

- Bandwidth is Important
  - Allows sufficient headroom for 3rd and 4th harmonics
  - Reduces path impact on jitter

Test Challenge!

HOW FAST IS YOUR SOCKET?
Old Way: *Opens & Shorts*

- Test for Open and Short conditions on each pin
  - Typical DC measurements of voltage and current
- Great for basic wiring and gross errors
- Will not detect Bandwidth or impedance problems

**CONCLUSION:**
Informative for gross errors, but won’t catch other more critical errors

Old Way: *Network Analyzer*

- Measuring Link Bandwidth Requires:
  - Network Analyzer for S21 parameters on each pin
  - Shorted die for round trip bandwidth
  - 500 measurements for 1000 pin device

**CONCLUSION:**
Great result, but impractical for most cases
Oh...by the way...

Measure BW at 3dB point

Works great on linear systems…but…

Look at the entire link model…

Non-Linear Effects are more important than the 3dB point!

Conclusion:
Not so great on real-world systems!
Old Way: Oscilloscope

- Measure Eye Diagram
  - Use high bandwidth repetitive sampling oscilloscope
    - Capture waveform contour to quantify relative transmission link performance
    - Can identify good paths from bad paths
  - Measure Each High Speed Signal
    - Pin counts over 500 pins
    - Test Time per pin >>20 sec

Old Way: Oscilloscope (cont.)

Conclusion:
Great Voltage vs. Time comparison, but impractical for most applications
Old Way: TDR

- Measure line length of each pin
  - Requires sampling oscilloscope and high bandwidth pulse generator
  - Determine length of each trace, including socket
  - Compare skew results to known good setup
- Measure each high speed signal

Conclusion:
TDR can find opens and shorts, but not effective for high bandwidth applications

Old Way: Software

- Use bus protocol to predict pin failure by coding patterns and transmitting them onto the bus
- Can detect certain pin failures at speed
- In-system testing
- Drawbacks
  - Code intensive/Proprietary software
  - Some uncertainty determining a local or remote pin error
  - Limited signal pin coverage
  - Lack of testing capabilities defined in the protocols (ie. DDR2, HyperTransport)
Risks of Current Methods

<table>
<thead>
<tr>
<th>Method</th>
<th>Risk Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Open/Short Socket Tester</td>
<td>Not enough test coverage</td>
</tr>
<tr>
<td>Network Analyzer</td>
<td>Too time consuming</td>
</tr>
<tr>
<td>Oscilloscope</td>
<td>Too time consuming</td>
</tr>
<tr>
<td>TDR</td>
<td>Too time consuming</td>
</tr>
<tr>
<td>Software</td>
<td>Low pin coverage</td>
</tr>
</tbody>
</table>

**Conclusion:** Time to shift paradigms!

Paradigm Shift

- **What is needed:**
  - Need to test as much as 500 pins for bandwidth
  - Need to test beyond 800MHz Bandwidth
  - Need to test reliability of socket in the development phase before production release

- **Why?**
  - Sockets begin to lose bandwidth over time from repetitive insertions and environmental breakdown
  - Lower bandwidth signal paths will reduce yield
  - Remove guess work from determining a failed socket in production
  - Reduce cost in socket development
Paradigm Shift (cont.)

• A Method for Measurement:
  – Measure Eye Opening on each pin using parallel BERTscan technique
  – Sweep Carrier Frequency to identify any reflection nodes or other filter functions.
  – Perform measurement on all pins simultaneously

Result:
- Bandwidth estimation on over 1K pins in less than 10 min.
- Pass/Fail result correlates to real-world performance

Background: BERTscan Theory

• Measure Bit Error Rate (BER) at various delays from Center of Eye
• Plot BER as a function of delay from Center
• Extrapolate Gaussian Region to 0.5 BER for Deterministic Jitter

Deterministic Jitter (DJ) = DJL + DJR
Real-World BERTscan Data

- PRBS $2^{23}$ Pattern - 15” & 45” Traces
- (3.125Gbps Data Rate)
- Eye Closure as a Function of DDJ

BERTscan Graph Analysis

- Socket-induced DJ can be simulated by increasing the trace length
- These data show correlation between decreased bandwidth and increased DJ
- Left and Right DJ are measured at the intersection with .5BER
- Data-Dependent Jitter (DDJ) is the only component of DJ present in our system
- Random and Periodic Jitter are held constant
- Marginal socket continuity will be visible as increased DJ outside the known good range
Conclusion

• Deterministic Jitter measured through socket quantifies Bandwidth Effect on real data patterns at data rate of target application

• No interpolation is needed

• Please contact the authors for additional data that was not available at press time.
OVERVIEW

- Trends in semiconductor industry driving burn-in socket technology.
- Modeling complex systems- defining the environment and constraints of the package undergoing burn-in.
- Analysis using finite element computational tools.
- Interpretation of results and incorporation into design.
CONCEPTS: "When America runs on bigger the better philosophy, our communication tools are getting ever smaller…….

INTRODUCTION

BURN-IN CHALLENGES - SHRINKING SILICON AND PACKAGES

Packaging Trends:
• Extremely small and thin packages.
• High I/O count bumped and LGA.
• 0.65mm pitch and below.
• Bare die and POP style packages.
• Soft mold compound.
CONTACT OPTIONS

- Transition from popular “pinch” style contact system to
  “compression style” contact system.

<table>
<thead>
<tr>
<th>Contact System</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Metal Pinch Contact</td>
<td>Transition to popular “pinch” style</td>
</tr>
<tr>
<td>Spring Probe</td>
<td>High force clamping mechanisms required</td>
</tr>
<tr>
<td>Helical spring</td>
<td>Typical contact force range</td>
</tr>
<tr>
<td>Buckling beam</td>
<td>Preference for open top to enable auto-loading</td>
</tr>
</tbody>
</table>

0.65mm pitch and above
0.65mm pitch and below

PACKAGE CLAMPING- OPEN TOP SOCKETS

- Compression style contact system requires high force clamping mechanisms.
- Typical contact force of 5~15g during burn-in.
- 200~500 I/O packages can see anywhere between 1kg to 7.5kg
- Preference for open top to enable auto-loading limits clamping surface
UNDESIRABLE EFFECTS OF BURN-IN

• Burn-in is an elevated temperature, long duration process in which the package is undesirably stressed by the loadings of the clamps and large number of electrical contacts.

• These loadings can cause distortion of the package and stress the circuitry on silicon.

• The extended duration of these conditions can cause continual deformation (creep) of the softer materials in the package like PCB, over mold compound etc., leading to possibly significant permanent change of shape of the package even when the high temperature and forces are removed.

• This condition can render the package useless.
Understanding Impact of Burn-In Sockets on Fragile Semiconductor Packages using Finite Element Analysis
BiTS Workshop 2007, March 11-14

**EFFECT OF STRESS AND TEMPERATURE ON PACKAGES**

- Need for understanding stress, stain and creep effects for packages/dies.
- Defining acceptable limits of stress and deflection.
- Need for robust, open top, ZIF automated solutions

**BURN-IN SOCKET REQUIREMENTS**

- Temperature: Up To 150 C
- Life: Up to 10,000 Cycles
- Resistance: Less Than 1 ohm per pin
- Acceptable Capacitance & Inductance
- Auto Loading Capabilities
- Acceptable Witness Marks
- No Damage To Die Or Package During Burn-in
DESIGN AND QUALIFICATION CYCLE

- Requirements
- Design
- Engineering analysis
- Prototype and qualification
- Production

Contact system, clamping mechanism, socket outline, etc.

ENGINEERING ANALYSIS

Finite Element Analysis (FEA) computational tools:

Non-linear analysis shows reduction in max. out of plane silicon deflection from 59 to 22 microns by increasing clamping surface area by 40%
**ENGINEERING ANALYSIS**

Finite Element Analysis (FEA) computational tools:

![Non-linear analysis](image)

Non-linear analysis shows reduction in max. out of plane silicon deflection from **85 to 32 microns** and stress by **24%** by moving support location.

---

**ANALYZING AN IC PACKAGE**

- Finite Element Analysis (FEA) is a powerful tool for accurately computing the physical response of a system when the geometry, boundary and initial conditions as well as the material properties are known.
- The material properties are often the limiting factor in the ability to perform a highly accurate analysis.
ANALYZING AN IC PACKAGE

For the class of problem in this presentation, the elastic properties may be known or can be measured, but the creep properties are not known and will be very difficult to measure.

• The package is a composite structure, with each material zone having its own properties.

MODELING

Modeling requirements:
• High temperature mechanical and creep properties of IC.
• Dimensions and x, y, z layout of the various layers.
• Contact force distribution.
• Clamping locations.
• Constraints that limit buckling or bending of the package.
MODELING

Modeling Concerns:
- Lack of good structural data on packages.
- Availability of mechanical properties at elevated temperatures.
- Creep properties.
- Composite material behavior depends on the type of attachment between layers.

MODELING

Building a good model:

- Empirical force-deflection data of composite structure using simple loading techniques
- Modeling the experiment using available properties of materials
- Apply actual loads, Constraints and temperature to the package as experienced in the socket during Burn-in
- Refining material properties to match creep results from the models to the empirical data
EMPIRICAL DATA EXTRACTION

- Three point bend test used to measure the force displacement response → Stiffness
- Fixed displacement extended time testing to measure the force decay → Creep properties of composite
- Image above shows FEM for quarter symmetric model. Package consists of FR4 substrate, silicon die, over mold compound.
- Contact conditions are used where package interfaces center shaft (where load is applied) and the bottom support shelf.

EMPIRICAL DATA EXTRACTION

- The force decay curves above follow a power law in time.
- This suggests that a simple power law representation of the creep strain can be used: \( \varepsilon_C = a_0 \sigma^{a_1} t^{a_2} \)
- Through iteration we arrive at the following effective creep constants for the given composite structure: \( a_0 = 7.0 \times 10^{-5} \), \( a_1 = 1.2 \), \( a_2 = 0.15 \).
- The FEA results match the experimental results well.
- Apply these creep properties to package when loaded in socket.
ANALYSIS- CREEP MODELS

Advanced features of our modeling and analysis:
- 3D Contacting surfaces
- Creep material model
- Non linear large displacement analysis
- Variable force contacts
- Computational and empirical properties extraction

- Model above shows the selected package with linear springs to represent contacts and cylindrical latches to apply the loading.
- Analysis uses elastic properties for Si and the derived creep constants at 125°C. A 40N load is applied for 4 hrs.
- Large displacement formulation using creep material model and 3D contacting surfaces, accounts for creep decay and force reduction in the contacts.
ANALYSIS- CREEP MODELS

- Image to the left shows deformation of package over four hours of loading followed by unloading to give permanent deformation.
- FEA results of 90 um permanent deformation (creep) compared well with measured average of 96 um.

Original design showed 90 micron out of plane permanent deflection

ANALYSIS- CREEP MODELS

- To reduce the deflection, the latches were moved 0.65mm inwards as shown on the image to the right.
- Moving the latches inward by only 0.65mm shows a large improvement on the permanent set. FEA results of 32um deflection compared well with measured average of 42um.
- FEA can make a useful prediction of the performance of the package in actual socket conditions.

Improved design showed only 32 micron out of plane permanent deflection
ANALYSIS- HIGH TEMPERATURE DEFLECTION MODELS

- Simulations showed that a package with large die on a substrate would experience excessive elastic deformation under certain socket loading and 125C.
- Symmetric ¼ model constructed as shown at left.
- Maximum deformation of 140 um estimated using FEA.
- Pressure plate is allowed to rotate about axis of shaft
- Therefore no resisting moment to keep package flat

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ANALYSIS- HIGH TEMPERATURE DEFLECTION MODELS

- New latch shown on left where shaft location is moved inboard with a corresponding inward contact point.
- Total package out-of-plane deformation reduced to 60 um concentrated toward edge. Die located in the center saw a 8um deflection.
- The shaft location is the key factor.

60 micron out of plane deflection concentrated towards edges

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ANALYSIS- HIGH TEMPERATURE DEFLECTION MODELS

• On the right, latch was modified to add a “foot” toward the package edge.
• Out-of-plane deformation reduced to 55 um, However die region deflection increased to 16um.
• Force applied by “foot” creates moment and causes additional rotation of latch \( \Rightarrow \) less force on die and more bending in that zone.

55 micron out of plane deflection more distributed on package.

Q & A
Contact Resistance is Sexy Again

2007 BITS Workshop

Morten Jensen / Tim Swettlen
Morten.s.jensen@intel.com Tim.Swettlen@intel.com swettlen@yahoo.com

Agenda

- Impact
- Trends and definitions
- Beyond the theory
- Measurement setup
  - System fundamentals
  - Required Support hardware
- Intel’s Best Known Method
- Summary
Impact of Contact Resistance

- Socket level Contact Resistance impacts Intel in three ways
  - Limits our ability to deliver power to the DUT
  - Final test ≠ OEM level
    - Over- or under-kill at final test
  - Changes with cycling, forces test environment to drift with time/cycles of the socket

Historical trending

Key Message: Resistance between package & PCB has dropped, but slowed in the last 2-3 years. Extreme applications at or near bulk pin resistance
**Power Integrity or Signal Integrity?**

**Power Integrity:**
- Target of $Z(f) \rightarrow 0$ ohms
  - Zero real (resistive) loss
  - Zero delay (inductive) loss
- Drives Resistance needs

**Signal Integrity:**
- Target of $Z(f) \rightarrow 50$ ohms
  - Zero reflection at interface
  - Zero attenuation along path
- **Does not** drive res. needs

$$Z = \sqrt{\frac{R + jwL}{G + jwC}}$$

**Definitions**

- **Total resistance**
  - Sum of resistances from test board to DUT

- **Bulk resistance**
  - Natural resistance of a solid, geometry-defined medium

- **Interface resistance**
  - Resistance between interfacing components
  - Comprised of a constriction resistance and a film resistance

---

Schematic diagram of electrical interface [2]
Controllable Variables

- **Bulk resistance:**
  - Material resistivity (\(\rho\))
    - Resistance proportional to resistivity
  - Geometry (L, A)
    - Resistance inversely proportional to cross-sectional area and proportional to length of a given contact geometry

\[
R_{\text{bulk}} = \rho \times \frac{L}{A}
\]

![Bulk Resistance vs. geometry](image)

- **Interface resistance:**
  - Normal force (F)
    - Increasing force reduces resistance
  - Effective resistivity (\(\rho\))
    - Lower resistivity reduces resistance
  - Material hardness (H)
    - Softer material reduces resistance

\[
R_{\text{int}} \approx C\left(\frac{\rho_1 + \rho_2}{2} + \rho_1 d_f (H/F)\right)^{1/2} + \rho_{\text{film}} (H/F)^{0.5}
\]
Controllable Variables

- Interface resistance
  - # of interfaces
    - Serial interfaces in path can increase total resistance significantly
  - Redundant contact (design)

- Contact tip geometry
  - Reducing contact tip area can reduce film resistance in interface
    - Higher pressure to penetrate film

Constraints and Challenges

- Typical Design constraints
  - Force limitations (per contact)
    - Socket contacts << 100gf to avoid package stress
  - Physical size/geometry
    - Driven by device layout and electrical requirements

- Challenges
  - Interfacing test board / device properties
    - Resistivity, hardness, flatness, etc
  - Cleanliness of test board / device
    - Film resistance!
  - Corrosion and wear
How Intel has chosen to define CRES

- CRES will be defined as the real impedance added to the conductive path between the PCB pad and package contact for one pin
  - CRES includes PCB capture pad to contact interfacial resistance
  - CRES includes native resistance of contact under normal load force
  - CRES includes contact to package pad resistance

But how do you measure this?

- Low resistance measurements (< 10 ohm) are subjected to lead resistance impacts [3]
  - 4-Wire techniques minimize this impact

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2-W DMM

<p>| | | | |</p>
<table>
<thead>
<tr>
<th></th>
<th></th>
<th></th>
<th></th>
</tr>
</thead>
<tbody>
<tr>
<td><code>V_M</code></td>
<td><code>V_R</code></td>
<td><code>R_PIN</code></td>
<td><code>R_L</code></td>
</tr>
<tr>
<td><code>V_M</code></td>
<td><code>V_R</code></td>
<td><code>R_PIN</code></td>
<td><code>R_L</code></td>
</tr>
</tbody>
</table>

Measured Res = \( V_M = R_S + 2 \times R_{LEAD} \)

Actual Res = \( V_R = R_S \)

Measurement topologies

Pro’s
- Very close to single pin results
- Measure every pin on the socket
- Higher sampling information

Con’s
- High channel count; 2x the pin count
- Very low readings; DMM’s resolution
- Complex PCB; more cost

Pro’s
- Low channel count
- Softens outliers

Con’s
- Requires routed package
- Requires trace subtraction

Beyond theory, practical concerns

<table>
<thead>
<tr>
<th></th>
<th>Life Cycling a socket</th>
<th>Heet of sockets</th>
</tr>
</thead>
<tbody>
<tr>
<td>End usage condition</td>
<td>Each socket &quot;sees&quot; 25-75k unique pristine packaged parts</td>
<td>Product requires 10 – 2000 sockets to support total volume</td>
</tr>
<tr>
<td>Lab validation concern</td>
<td>25-75k unique package simulators?</td>
<td>Cost &amp; Time of measuring 10 – 2000 sockets</td>
</tr>
<tr>
<td>Simple solution</td>
<td>Reuse device simulators</td>
<td>small sample of sockets, but tight limits &amp; every pin tested</td>
</tr>
<tr>
<td>Noise factor</td>
<td>Life of device simulator Topology of simulator</td>
<td>One outlier pin Stability of supply Pin lot-to-lot variation</td>
</tr>
</tbody>
</table>
A slide about surrogate packages

- Intel is studying numerous different types of device simulators
  - Conductive (8 flavors)
  - Daisy Chain and expired units

Outcome

- On LGA applications, we find it best to use Stainless Steel with Au or Ni/Au plating
  - Both value (mean) and spread (sigma) mirror the control units of expired product parts

Data collected @ 0, 5k, 20k & 50k. Presented data is from the 5k step. Treatments highlighted in Red support the hypothesis that their means are equal to the control (Target) mean. [4]
Key takeaways so far

- Dialing in Contact Resistance on a high volume platform is a multi-million dollar variable
- Today’s contact resistance targets require crisp definitions between the user and supplier
- Contact Resistance is predominantly a Power Integrity impact, not a Signal Integrity one
- There are few fundamental knobs to turn in the pursuit of optimized total resistance performance.
  - Largest gain seemingly w/ interface resistance
- 4 wire techniques must be used
- Mimicking end us conditions requires care in the selection of the device simulator and cycling

Our Measurement System and How We Use It
Best Known Standard @ Intel

PCB for routing to pins. Also emulates the PCB/socket pad.

Most 4-wire DMM with a cross point relay block can work.

Best Known Standard @ Intel

Cycle count

5 repetitive measurements spread @
[1-5]
[1000:1005]
[5000:5005]
[10000:10005]
[20000:20005]
[30000:30005]
[40000:40005]
[50000:50005]

Mechanical Cycling w/ no diagnostics
[6:999]
[1006:4999]
[5006:9999]
[10006:19999]
[20006:29999]
[30006:39999]
[40006:49999]

Totals 40 measured cycles

Totals 49,960 mechanical cycles
Best Known Standard @ Intel

Sensitivity to outliers is up to customer. We chose 5% at validation.

So at 50k, 95% of the pins are below 55.56 mΩ.

BestKnownStandard@Intel

Materials

- 1249 total Pins
  - Value: 0.24589
  - Value: 249.99

Values

- 1249 total Pins
  - Value: 0.24589
  - Value: 249.99

Cycle Readout

• Positives
  - Simple in theory
  - Most of the system is off the shelf hardware
  - Effort to prove it matches end use conditions
    • Still more to go
  - Open to scrutiny

• Negatives
  - Time from concept to data too long
  - Requires hardware to wrap around socket to test
    • PCB, device simulator, compression force
  - Currently no automation or standardization of cycling piece of the flow
Where do we go from here

- Intel will share the following documents
  1. Gage R&R DOE steps
     - Used to help gather a metrology system accuracy
  2. Reference design for resistance testing
     - May choose to match Intel and become qualified
  3. Reference metrology system details
  4. Reference device simulators and plating recipes
  5. Step by step validation testing

Key message, we are not contact physic experts nor do we wish to be. Our motivation is to make supplier results more meaningful so we can rapidly assess the fit of technologies to our needs.

Summary

- Contact Resistance is a widely used metric for sizing up, monitoring and validating a contact
- Today’s requirements require crisp terminology and metrology between user and supplier
- We are not experts, but we have studied and will share our Best Known Methods with the goal to narrow future definitions and measurement methods
THANK YOU!

References


