“Enabling High Volume Testing Of MCP Memory”
Ken Karklin — Agilent Technologies

“An Alternative Test For Verifying Connectivity On High Pin Count Devices During Burn-in”
Rick Larson, PE — Texas Instruments, Inc.
Bunny Gaab — Enplas Tesco, Inc.

“Minimizing Spring Probe Operational Cost Using Optimized Maintenance Techniques”
Erik Orwoll — Nu Signal LLC
Enabling High Volume Testing of MCP Memory

Efficiency Initiatives Session

2006 Burn-in and Test Socket Workshop
March 12 - 15, 2006

Ken Karklin
Test Cell Integration Manager, MTS

Outline

• Mobile Memory / MCP Growth
• Need for More Effective Solutions
• The Matrix MCP Solution
• Massive Parallelism = Massive Connections
• Complex Electromechanical Challenges
• Achieving Signal Performance at the DUT
• Handler Roadmap & Conclusion
Mobile Memory / MCP Growth

- Fueled by the mobile device market
- These Multi-Chip Packages (MCP) devices combine multiple memories in one stacked unit
- By 2009, nearly ½ of all FLASH memory will destined for a MCP

MCP Growth (continued)

![Graph showing MCP and Flash Revenue growth from 2004 to 2009](image)

- MCP Revenue
- Total Flash Revenue
- MCP % Total Flash

Data: iSupply
MCP Growth (continued)

High Mix/Low Volume vs. Monolithic Memory
... and likely to stay that way!

- “We counted 200 million MCPs shipped in 2003, and that number could easily exceed 500 million in 2008.” – Richard Gordon, Gartner/Dataquest (Dec ‘04)

- “MCP unit shipments should remain in the 600-800 million range over the 2005-09 forecast period.” – iSuppli (Feb ‘05)

Multiple Types of Memories in MCPs
Multiplying the Complexity of the Test Problem

- Requires a 123 pin/Site tester with 200Mb/S performance and Flash test capability.
Need for More Effective Test Solutions

- Traditional Memory Tester Operational Flow Applied to MCP

  ![Diagram of test flow]

  - DIE 1 Test
  - DIE 2 Test
  - DIE 3 Test
  - ...
  - INSERTION + HIFIX
  - INSERTION + HIFIX
  - INSERTION + HIFIX

- Alternative? Highly custom HiFix with << //
  - Thousands of discrete relays, cooling, cost, << reliability

One MCP focused Solution:

- V5500 = 4096 I/O
- Matrix = x 6 resource multiplier
- Effective **24,586** I/O at test plane
... Matrix Interface Solution (continued):

- Each I/O channel selectable switching to any/all of 6 DUT resource locations
- Alternatively, switch any DUT resource to one of 8 programmable voltage levels
- MCP tested in one insertion – Global test program execution

Matrix Interface Application Test Flow
Combine Into One

ONE INSERTION ONE FIXTURE

Step 1: Development
Global Resource of MCP

Step 2: Rename of local resource to resolve name conflict
… Matrix Interface Solution (continued):

- HW Core of Solution:
  - Kiowa Custom ASIC
    - Located ~2" from DUT
    - Low leakage
    - High Bandwidth
  - Ultra High Density Interconnect

768 I/O
+ +
Per Slice
Is This Really Different?
Haven’t we been doing this with relays for years?

• How is this different than what has been done with relays?
  • All channels can be switched: equivalent ~60k relays
  • Universal: doesn’t increase cost of each load board
  • Relays don’t provide high performance fan-out
  • Provides ability to maintain state of switched pins

• Why not put this on the load board?
  • Reliability becomes impossible
  • Cost, Lead-Time
  • Only manufacturable way to do in load-board/Hifix is to dramatically reduce parallelism

... Matrix = Parallelism @ DUT Plane

• x320 DUT // MCP for TW320 Handler Pictured
• Up to 512 DUT Possible
• Only limited today by handler solutions
Matrix = Massive Resources at DUT Plane … and Big Electromechanical Challenges

- >55,552 total contacts @ ~40gf
- 5 ton total force across minimal stroke
- Leverage 4-bar linkage w/ cam x 2 DUT attach planes
- Manually actuated simple and robust

Matrix Thermal Challenges Addressed

- Designed / tested for up to 150C test temperature
Electromechanical Challenges: … Contact Performance a *Statistical* Game

- Reliability, Modularity, Replace-ability
- Integrated Commodity Interposer Technologies

Matrix Socket Board Density

- Alignment challenges solved across temperatures
Matrix Interface Performance

- DC Performance (ohms):
  Including Flex, Interposer Contact to DUT Board

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
<th>Portion</th>
<th>% Actual</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lower Spec Limit</td>
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<td>Upper Spec Limit</td>
<td>0.6</td>
<td>Above USL</td>
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</tr>
<tr>
<td>Spec Target</td>
<td>0.6</td>
<td>Total Outside</td>
<td>0.0000</td>
</tr>
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</table>

Overall, Sigma = 0.03419

Matrix X-Mission Line Performance

- Zo Performance (ohms):
  Including Flex, Interposer Contact to DUT Board

<table>
<thead>
<tr>
<th>Specification</th>
<th>Value</th>
<th>Portion</th>
<th>% Actual</th>
</tr>
</thead>
<tbody>
<tr>
<td>Lower Spec Limit</td>
<td>47.5</td>
<td>Below LSL</td>
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<tr>
<td>Upper Spec Limit</td>
<td>52.5</td>
<td>Above USL</td>
<td>0.0000</td>
</tr>
<tr>
<td>Spec Target</td>
<td>52.5</td>
<td>Total Outside</td>
<td>0.1674</td>
</tr>
</tbody>
</table>

Overall, Sigma = 0.85734
Driving Signals Through Matrix

Signal Path With 1:6 Matrix

Handler Roadmap

- Supporting available and evolving solutions
- Each requires optimized electromechanical assembly

Editor’s Note
Summary

– MCP growth is substantial
– MCPs create test complexity
– The matrix MCP provides an efficient, low COT solution
– Extreme Parallelism challenges solved:
  • Novel ASIC design / placement
  • Electromechanical innovation
  • Breakthrough interconnect technology
– Integrate to multiple handlers
– Enabling the mobile-device MCP memory explosion!

Acknowledgements

– Sanjeev Grover, Agilent, for tireless debug, data taking & superb high density electrical design
– Todd Sholl and Steve Bellato, Agilent, for innovative mechanism design, debug and product validation
– Vick Kovacevic, Ben Morris and Kurt Gusinow, for helping me to understand the economic dynamics on MCP test
– Mirae Corporation for their cooperation
– TechWing Co. Ltd, for their cooperation
AN ALTERNATIVE TEST FOR VERIFYING CONNECTIVITY ON HIGH PIN COUNT DEVICES DURING BURN-IN

2006 Burn-in and Test Socket Workshop

Rick Larson
Texas Instruments, Inc.

Bunny Gaab
Enplas Tesco, Inc.

Agenda

- Objective
- Test description
- Pattern development & evaluation
- Test results
- Set up requirements
- Advantages & disadvantages
- Conclusions
Objective

- To find a method for quickly isolating a contact related failure at a burn-in socket position for a minimal amount of cost
- To be able to verify connectivity of a high-pin count DUT at burn-in temperatures

Test Used

- JTAG Boundary Scan
  - IEEE 1149.1 Standard Test
  - Typically used by board manufacturers for verifying IC-to-PCB interfacing
Boundary Scan Diagram

In

Device Logic

OUT

Boundary Scan Cell

Pass Example

IN-1 1

B-Scan Cell-1

1

IN-2 0

B-Scan Cell-2

0

TDO

Fail Example

IN-1 1

B-Scan Cell-1

1

IN-2 0

B-Scan Cell-2

0

Disconnect or short

TDO

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Paper #2
Test Set Up

- **Device**
  - Niagara (Sun Microsystems)
  - 1933 pin LGA with a 1mm pitch (51mm body)
- **BI Stress Needs**
  - Scan & BIST (~100 pins)
- **Burn-in oven**
  - MCC HPB-3
- **Socket**
  - Clam shell compression mount socket

Pattern Development Flow

1. Modify BSDL file for BI pins
2. Obtain/create boundary scan pattern generator
3. Create boundary scan test pattern (TDL, STIL, VCL, etc.)
4. Translate pattern into BI pattern format (VEC)
Pattern Evaluation Flow

Enable error log mode on BI oven

Execute pattern

Error Log File

- **BIB id**: 6465
- **zone**: 0
- **slot**: 6
- **Lot Id**: H1
- **QV this run**: 0
- **Init SI**: 1
- **# of socket's following**: 1

Socket: B1
Socket Board ID: 0
DUT Serial Number: *

Pattern Evaluation Flow

- **Translate address fail location to DUT pin from table**

- **Data**
- **State**
- **Pin Name(s)**
- **Pkg Coord**
- **Drv/Rcv Number**

<table>
<thead>
<tr>
<th>ELOG Addr</th>
<th>Data State</th>
<th>Pin Name(s)</th>
<th>Pkg Coord</th>
<th>Drv/Rcv Number</th>
</tr>
</thead>
<tbody>
<tr>
<td>7821</td>
<td>H</td>
<td>DRAM1_DQ_43</td>
<td>sD24</td>
<td>AK42 79</td>
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<td>7829</td>
<td>L</td>
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<td>H</td>
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</tr>
<tr>
<td>7889</td>
<td>L</td>
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<td>7891</td>
<td>H</td>
<td>DRAM2_DQ_89</td>
<td>sD27</td>
<td>BD3 76</td>
</tr>
</tbody>
</table>

Merge output information to database
Quickly identified broken isolation resistors on burn-in board

Enabled socket supplier to isolate exact contact location of problem sockets during prototype evaluations...
Development Results

- ... analyzing only 2-5 pins out of the possible total of 1933 pins per socket.

Production Results

- Majority of failures attributed to parts being dropped during manual loading & unloading of BIBs
Repair Time Savings

<table>
<thead>
<tr>
<th>Old Flow</th>
<th>New Flow (w/ b-scan test)</th>
</tr>
</thead>
<tbody>
<tr>
<td>Test technician marks failing socket w/ disposition tag</td>
<td>Test technician marks failing socket w/ disposition tag</td>
</tr>
<tr>
<td>Repair technician narrows fail to a group of potential pins</td>
<td>Repair technician looks up failing pin location(s) on database</td>
</tr>
<tr>
<td>Repair technician diagnosis fail with meter and/or oscilloscope and performs repair</td>
<td>Repair technician confirms failing pin and performs repair</td>
</tr>
</tbody>
</table>

Total Repair Time ~ 0.5hr to > 3hr

Total Repair Time ~ 0.2hr to 0.5hr

Boundary Scan Requirements

- Designed into device
- Burn-in oven that can log failing output address locations to a pin channel
- Boundary Scan Description Language (BSDL) file
- Translators –
  - create JTAG pattern
  - convert pattern to burn-in oven format
  - modify error log output to device pin name & location
Advantages

- Enables a fast method for identifying contact related problems
- Test can be performed at burn-in conditions with actual devices
- No additional equipment costs required

Disadvantages

- Not able to verify connectivity on JTAG pins (TDO, TDI, TMS, TCK, TRST) or other pins not connected to boundary scan chain
- Initial development time to create custom pattern & translators
Conclusions

- Using a boundary scan test during burn-in has been found to be a valuable tool for quickly identifying contact problems during burn-in development.
- Performing a boundary scan test during production checkout has enabled BIB repair times to decrease by as much as 6x.

Future Development

- Setup boundary scan test for non-driven IO pins.
- Add in real-time translation and reporting of error log results during program executions.
Acknowledgements

- Bunny Gaab - Enplas Tesco (socket)
- Micro Control Company (burn-in oven)
- Robert Young – TI (BI technician)
Minimizing Spring Probe Operational Cost Using Optimized Maintenance Techniques

2006 Burn-In and Test Socket Workshop
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Erik Orwoll - Nu Signal LLC

Discussion Points

❖ Where Do Probes Fail?
❖ Failure Modes / Causes
❖ Options To Address Failures
❖ Production Yields
Failure Points

- PCB Pad
- Spring Probe / PCB Interface
- Internal Probe Wear & Fatigue
- DUT Interface

PCB Pad Wear

Abrasive Wear
Gold and Nickel Layers Compromised

Initial
Re-Plated

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DUT Interface
Failure Modes

- Contamination
- Mechanical Wear
- Mechanical Damage

DUT Interface
Contamination Sources

- Solder
- Resin
- Glycol
- Flux
- Dirt
- Device Binders / Adhesives
- Residue from alcohol and cleaning products
DUT Interface

Crown Point Witness Marks (Ambient)

DUT Interface Contamination

Solder Contamination & Flattened Crown Points

Impregnated Resin

Damaged Point

Oxidized Solder
Maintenance Methods Observed

- **Mechanical Cleaning**
  - Abrasive Pads / Abrasive Media
  - Brushing
  - Adhesive (Sticky) Pads
- **Chemical Contact Cleaners**
  (Oils result in device contamination)
- **Ultrasonic**
- **Air Hose / Air Blast**

Brush Cleaning

- Removes surface oxides
- Damages plating

Solder Contamination | Solder Removed
--- | ---
Exposed Copper | Exposed Nickel
Surface Scratches |
Solder Diffusion & Intermetallic Au-Sn Compound Formation

Source: Materials Science and Technology, September 1992, Vol. 8

Solder Diffusion & Intermetallic Compound Formation

Solder Contamination
QFP Contact

Solder Extracted
Intermetallic Compounds Exposed

Non-Conductive Crystalline Structure
Gold Loss - Contact Tip

Spectrum Analysis
Contaminated

Restored

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Probe Performance

144 Pin BGA Socket

Use Cycle

Devices Tested

Brush Clean

Metallic Restoration

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Maintenance Fixtures

Fixture Allows Socket To Remain In Use
Probe Maintenance Performed Off-Line

March 2006

Thank You!

March 2006