“Development Of Computational Model And Measurement Of Maximum Current Capability For Microprocessor Sockets”
David W. Song, Ashish Gupta, Chia-Pin Chiu — Intel Corporation

“Lumped And Distributed Equivalent Circuits For Test Sockets”
Gert Hohenwarter — GateWave Northern, Inc.

“Contactor Characterization Of RF Test/Burn In”
Ling Li Ong, Tim Swettlen — Intel Corporation

“Differential Impedance Characterization Of Test Sockets”
Eric Bogatin, Kevin DeFord, Meena Nagappan — Synergetix

COPYRIGHT NOTICE
• The papers in this publication comprise the proceedings of the 2006 BiTS Workshop. They reflect the authors’ opinions and are reproduced as presented, without change. Their inclusion in this publication does not constitute an endorsement by the BiTS Workshop, the sponsors, BiTS Workshop LLC, or the authors.
• There is NO copyright protection claimed by this publication or the authors. However, each presentation is the work of the authors and their respective companies: as such, it is strongly suggested that any use reflect proper acknowledgement to the appropriate source. Any questions regarding the use of any materials presented should be directed to the author/s or their companies.
• The BiTS logo and ‘Burn-in & Test Socket Workshop’ are trademarks of BiTS Workshop LLC.
Development of Computational Model and Measurement of Maximum Current Capability for Microprocessor Sockets

David Song    Ashish Gupta    Chia-Pin Chiu

ATD Design Process Development
Intel Corporation, Chandler, AZ

Collaborators:
Suzana Prstic    Yongmei Liu
Todd Young    Seth Reynolds
Tom Paddock

Agenda

- Motivation
- Introduction to Socket Thermal Analysis
- Review of Previous Status
- Improved Numerical Model for Contact Temperature Prediction
- Improved Experimental Model Validation
- Key Summary
- Glossary
Motivation

- Increasing need to quantify current per pin.
  - Higher local joule heating.
  - Higher socket contact temperature.
  - Accelerated increase in electrical contact resistance through product life.

- Need to more accurately evaluate socket contact temperature at use-condition.
  - Large uncertainty → Low confidence
  - Small uncertainty → High confidence → More margin

- Intel is constantly driving methodology improvements for determining socket temperature.

Socket Thermal Risk Assessment

- Socket Thermal Risk Assessment is governed by: 
  **Maximum allowed contact temperature** (Tc,max) 
  **Need Risk assessment** against Tc,max at the product boundary conditions.

- Current Method for Socket Thermal Risk Assessment:
  - Correlate Tc,max to the maximum board temperature (Tboard,max) → Easier to measure & validate.
  \[ Tb,max = Tc,max - \Delta T \text{ (For given conditions)} \]

- Tools:
  - Finite Element Model (FEM) Simulation (ie, ANSYS)
  - Infrared (IR) Experimental Characterization
Review of Previous Status

- Previous experimental result (BiTS 2005) showed that package substrate temperature (Tsub) has a large impact on socket contact temperature.

- **IR Thermometry:**
  - Socket pin temperature profile at strategic data points (Ipin, Tsub, Tb)
  - **Empirical model (Data fit)**
  - Tool to determine $\Delta T$.

![Cross-cut Socket IR Image](Image 1)

![Thermal TV](Image 2)

Latest FEM Model

- Previous FEM model assumed adiabatic condition at the contact interface:
  - No substrate effect $\Rightarrow$ Big caveat.

- Current FEM model covers a single-pin footprint, including (top to bottom):
  - Substrate Tile
  - LGA land
  - Contact Interface
  - Socket pin
  - Solder ball
  - Motherboard Tile

- **Objective:** Determine contact interface temperature as a function of current per pin, substrate, and board temperature.
Validating FEM Model

Match temperature at two points on the socket pin between model & experiment under specific range of conditions.

Caveat: Comparison done at low contact resistance.

Finding Tb,max

- Increase contact resistance in the modeling domain.
- Run ANSYS model DOE at different Tsub, Tb, and Ipin.

Model Output:
- Tc for each simulation
  \[ Tc = f(Tsub, Tb, Ipin) \]
- Sensitivity of Tc to Tb at a given Tsub & Ipin

Calculate Tb,max at the given:
- Tsub
- Ipin
- Tc,max

\[ Tb,max = f(Tsub, Tc,max, Ipin) \]
Risk Assessment:

\[ T_{b,\text{max}} \text{ vs. Use-Condition } T_b \]

- Low Risk
- High Risk

Use-condition \( T_b \) (Qualitative)

\[ I_{\text{pin}} (A) \]

Compare to:
Use-condition motherboard temperature

Sample IR image of motherboard underside.

Additional Experiment

- Key extension from previous experiment (BiTS 2005):
  - Physically achieve high electrical contact resistance (\( R_c \)) for realistic worst-case at the end of life.
  - Real-time monitoring of thermal boundary temperature (Directly from IR measurement)

Controlling \( R_c \) extends the applicability of empirical model to sockets of different designs.
Experimental Validation (Cont’)

Methodology Overview:
Conduct two separate DOE’s:
1. Low contact-resistance socket
2. High contact-resistance socket

Sample preparation:
Cross-cut, black-coat & wire the socket / board.

Technical Challenge: Single-Pin Resistance
• Need to measure the electrical resistance of a single pin, in order to correlate to temperature measurement.
IR Imaging

- Monitor:
  - Substrate
  - Contact
  - Pin pivot
  - Pin body (covered by molding)
  - Solder Ball
  - Motherboard

Socket-Pin Temperature Profile

- Higher contact interface resistance results in larger joule heating at high current per pin → hotter contact interface.

- Graph showing temperature profiles for different currents.

- Black-coated Socket / Board Cross-section

- IR Camera Field of View

- IR Image

- IR Imaging
Ongoing Activity: Extend FEM Model to Multiple Contacts

- FEM must capture the experimental boundary conditions: pin-to-pin interaction and environmental effects (like system airflow).
- The model can be used to study the placement of high current contacts.
- The model can be further used for socket thermal solution design and optimization.

Key Summary

- Socket thermal analysis has been significantly improved in both numerical modeling and experimental methodology.
- For numerical model, the effect of substrate temperature (very important) has been added and matched to the previous empirical model.
- New infrared-imaging experimental methodology incorporates significant improvements over the previous one (BiTS 2005), most notably the physical achievement and measurement of high-resistance socket pin.
- Improvements in methodology will increase confidence in critical socket thermal risk assessment and ultimately provide an increased margin in socket current capacity.
Glossary (Alphabetical Order)

BKM – Best known Method
DAC – Data acquisition and control
DOE – Design of experiment
FEM – Finite element analysis
IHS – Integrated heatsink
Ipin – Current per socket pin
IR – Infrared
\( \Delta T \) – Temperature drop between the socket pin contact interface and the local motherboard temperature.
Tb – Motherboard temperature
Tb,max – Maximum allowed motherboard temperature
Tc – Contact interface temperature
Tc,max – Maximum allowed contact temperature
Tsub – Package substrate temperature
TV – Test vehicle,
i.e. a mock-up processor/ socket/board set.
Lumped and Distributed Equivalent Circuits for Test Sockets

2006 Burn-in and Test Socket Workshop
March 12 - 15, 2006

Gert Hohenwarter
GateWave Northern, Inc.

Objectives

• Demonstrate uses and limits of different models
• Show performance potential and limits of
  – Loadboard with socket
  – Fast PCB
  – Loopback from a DUT onto a PCB
  – Straight thru
• Point out some pitfalls
• Place socket properties into application perspective
Equivalent circuit of a connection

Common representation:

- L – inductance of pin
- C12 – capacitance to neighbor(s)
- M12 – mutual inductance
- R – loss term

Simplified single pin models

- L - does not take capacitance to adjacent pin into account - typ. used for power/ground
- CL - one lumped capacitor to ground
- LC - one lumped capacitor to ground
- PI - two capacitors of C/2 value to ground
- TL - transmission line with distributed L and C

Example:
1 nH, 0.3 pF
57 Ohms, 17 ps
‘Physical’ configuration for the following simulations

One signal, multiple grounds

Equivalent circuits

These are the simplest equivalent circuits for the signal path possible. A full connection normally consists of a ground path as well.

The respective model is inserted between source and load
Insertion loss (SPICE simulation)

- Lumped models limited even at moderate frequencies
- Accuracy of element less significant at higher frequencies

Transmission (SPICE simulation)

- Time domain thru simulation of a 20 ps risetime step as observed at the load

The thru evaluation does not adequately show the differences between models.
Lumped vs. distributed models

- TD reflection model (SPICE) shows significant differences

Model applications

L - low frequencies - typ. used for power/ground

CL - low frequencies

LC - low frequencies

PI - moderate frequencies

TL - high frequencies, not suited for power and ground models
Simple inductance model

Two planes linked by an array of ground connections

Groundplane model

Pin inductance

Spreading inductance (groundplane)
Groundplane model

- Effective inductance depends on position of where current enters the interconnect
- Individual pin inductance is masked (at low speeds)

Spreading inductance = 0.1 nH assumed
PCB model

- Model contains lossy Tmlines and coax from tester to DUT plus interconnect discontinuities

PCB model

- PCB properties dominate response
- Model differences are insignificant

The example (measured response) only serves as a comparison. It is not modeled.
Fast PCB model

- Model contains a short lossy Tline, a high frequency loss term \((R_L C_L)\) plus interconnect discontinuities

![Diagram of PCB model]

Fast PCB model

- Socket properties dominate response
- Model differences significant

![Graph showing S21 response]

The example (measured response) only serves as a comparison. It is not modeled.
**Crosstalk model (freq.domain)**

- L model is inadequate (backwd= fwd)
- TM line predicts somewhat lower crosstalk

![Diagram of Crosstalk model (freq.domain)](image)

**Crosstalk model (time domain)**

- The ‘L only’ model shows the wrong trend for forward crosstalk
- All others show similar responses

![Diagram of Crosstalk model (time domain)](image)
Loopback model

- Signal enters interconnect through one contact and is returned through a second contact.

Loopback model

- Lumped models with coupling show large insertion loss.
Loopback model

• Eye diagrams predict system performance
• Source:

Random sequences of pulses are superimposed on top of each other

Loopback model

• Eye diagrams at 5 Gbps

LC

PI

TL
Loopback model

- Eye diagrams at 10 Gbps

Even the transmission line model is showing aberrations.

Loopback

- Performance limitation at elevated frequencies
  - Example (lab experiment)

Note the difference between measurement and model (slide 22). It is caused by the lack of ground return connections in the model.
Loopback
Simplified SPICE model:

- Causes for performance limitation at elevated frequencies:
  - Ground path, coupling to other connections and impedance transformation

Insertion loss as a function of frequency and electrical linelength (td):

Loopback model

- Additional causes for performance limitation at elevated frequencies:
  - Field distortion (parasitic elements, radiation)
Loopback model

- Performance limitation at elevated frequencies
  - Fields distorted
  - Multiple discontinuities
  - PCB loss/fringe/radiation contributions
  - Dependent on length of line between contacts
  - Ground return path disrupted

Conclusion

- Interpretation (significance) of parameters and their variations depends on environment a socket is placed in
- At elevated frequencies, TMline representations become imperative
- Pin performance at elevated frequencies can only be assessed in configurations that allow these frequencies to be reached
Contactor Characterization of RF Test/Burn In

Ling Li Ong
Tim Swettlen
Intel Corporation

Objectives

- Introduction of Pin Inductance Characteristics
- Discuss techniques of measurement with fixture and without fixture.
- Summary
Why is this an issue for Intel?

- Wireless hardware leverages the cost/performance of QFN type package
  - Vss (return) pin population becomes an optimization
- IEEE 802.11 a/b/g/n products require stable power up to the band of operation:
  - 2.4 GHz & 5GHz
- Therefore, Stable path to power supply through the QFN; well into 5 GHz range without over designing the socket

Introduction to Pin Inductance

Inductance can be explained with total number of magnetic field lines induced when current flows through conductor.

A) Partial self Inductance
   - Inductance of a single pin

B) Mutual Inductance
   - Influence of one magnetic field to another magnetic field
   - Pitch ↓, Mutual Inductance ↑

C) Loop Inductance
   - Total inductance induced when a complete loop of current path is formed.
   \[ L_{\text{LOOP}} = L_{\text{SELF1}} + L_{\text{SELF2}} - 2(L_{\text{MUTUAL}}) \]
Factors on Inductance: Pitch

Ansoft’s Q3D™ Modeling Result

\[ L_{\text{LOOP}} = L_{\text{SELF1}} + L_{\text{SELF2}} - 2(L_{\text{MUTUAL}}) \]

Key: Loop inductance depends on pitch

Factors on Inductance: # of pins

Ansoft’s Q3D™ modeling

- All pins have identical dimension
- 3 models have same pitch between power and ground pin

Key: Diminishing impact when adding more ground pins
Model usage

- 3D electrical modeling tools are good to quickly understand what happens when you change a given attribute … BUT …
- Time must be spent to validate key models with some form of measurement
- Complex models require finesse to utilize
  1. Simplify attributes when possible (cylinder for pin), or
  2. Model pieces of power path and stitch together
    - Even “small” QFN too complex for 3D elect. modeling

Model Stitching

- Like almost any modeling software, 3D electrical modeling can be broken into smaller pieces

Steps:
1. Parse the package into 3D friendly size blocks
2. Model each block only focusing on power and ground pins
3. Produce a inductance per block and summate for total impact
Objectives

- **Introduction of Pin Inductance Characteristics**
- **Discuss Inductance measurement techniques with and without fixture.**
- **Summary**

Measurement Flow

**Equipment List:**
- Network analyzer, Probe Station, Probe arm, Microprobe, Calibration Substrate.

**Measurement Steps:**
1. Attach appropriate microprobe to probe arm
2. Connect Network Analyzer to microprobe by coaxial cable
3. Calibrate microprobe with substrate.
4. Short Power and ground pin with shorted unit.
5. Start measurement on socket.

**Note:** Measurement repeatability was necessary to ensure result’s consistency.
Measurement without fixture

Step 1: Assemble test coupon (socket + shorted unit + hand clamp)
Step 2: Flip assembled test coupon to the back side
Step 3: Land microprobe on top of Power (Vcc) and Ground (Vss) pin

Why we need fixture?

1. Difficulty existed to measure large pitch
   - Gap between power and ground pin larger than the range where microprobe can cover.
2. For measuring group of ground pins
   - To closely reflect actual package topology.

Using fixture to compare measurement results with different ground pin topology.
Two types of fixture are needed: 1) Fixture Board 2) De-embedding Board

Key: Added inductance from fixture must be considered & minimized

Measurement With Fixture

- Socket Board current flow direction
- 1-port measurement

Hand Clamp

Shorted unit

Vcc Pin

Group of Vss pins

Power via

Fixture Board

Ground vias

Ground traces

Power trace

microprobe

Socket

Fixture Board

Flip

Measurement With Fixture
Measurement With Fixture

- **De-embedding Board**
  - To measure loop inductance contributed by fixture only
  - A closed current path is formed when customize trace shorts power pad to ground pad
    - 1-port measurement

---

De-embedding Concept

**Socket + fixture** = **Fixture**

**Socket only**
Smith Chart can be used to analyze results during measurement. It shows whether the contact is closed or open. It shows whether the contact is inductive or capacitive.

Equation to extract inductance:

\[
L = \frac{\text{imag} \left( S(1,1), 50 \right)}{2 \pi f}
\]

After post-processing, ADS can be used to graphically display "L" (inductance) versus frequency.

**Note:** Impedance is dominated by inductance, so the graph is approx. flat.
Summary

- Important to optimize total loop inductance even in low power RF DUTs
  - Balance total pins to meet needs, not exceed

- When measuring, only loop inductance can be directly measured

- When modeling, validate results with measurements and expect to

- Fixture can be built to overcome measurement limitations of wide pitch and group pins topology
  - Extra effort required to remove impacts of the added fixture

Questions?
Differential Impedance Characterization of Test Sockets

Eric Bogatin, Kevin DeFord, Meena Nagappan
Synergetix
Kansas City, KS
www.Synergetix.com

2006 Burn-in and Test Socket Workshop
March 12 - 15, 2006

Agenda

• What’s differential impedance
• What’s characterization mean?
• The Synergetix Method
• Current results
• Future directions
Differential Impedance

- Differential impedance is the instantaneous impedance the difference signal sees

$$Z_{\text{diff}} = 2 \times Z_{\text{odd}}$$
A Common Mis-Conception

“The return current of one line is carried by the other line.”

<table>
<thead>
<tr>
<th>When return currents overlap, second pin has the return current of the first pin</th>
<th>Signal to signal coupling &gt;&gt; signal to return coupling</th>
<th>Return path not important</th>
</tr>
</thead>
<tbody>
<tr>
<td>When return currents do not overlap, return current of each pin is in the return conductor</td>
<td>Signal to return coupling &gt;&gt; signal to signal coupling</td>
<td>Return path critical</td>
</tr>
</tbody>
</table>

Standardized Return Path Definitions

- 0a
- 1a
- 2a
- 4a
- 6a
What is Electrical Characterization?

Physical world

Behavior model: insertion loss, return loss

Electrical world

SPICE model: RLCGT matrix elements

SPICE Topology Circuit Models for Ideal Differential Pairs

- Option 1: ideal, lossless differential pair
  - Zodd, Zeven, DKeven, DKodd, Length

- Option 2: ideal differential pair with skin depth limited conductor loss

- Option 3: ideal lossy model based on RLG matrix elements
  - Includes dielectric loss, conductor loss, asymmetric impedance
  - Can be used to simulate all properties of a differential pair
  - Difficult to extract a “differential impedance”
Synergetix Characterization Method

Goals

• Simple, reproducible and generic for any probe configuration
• Unambiguously de-embed the fixturing
• Non-proprietary
• Circuit topology model with verified accuracy > 10 GHz
• Output a differential impedance that has meaning
• Provide differential insertion and return loss
• Use only 2 port VNA

Synergetix System Configuration

• Agilent E8363B VNA
• Megaphase high bandwidth cables
• GGB industries pico probes
• Synergetix custom test board
• Synergetix custom rf test socket
Probes and Test Board

Probe Configuration for 2a Pattern

Three measurement conditions of bottom plate:
- Open
- Short
- Thru

X ray image of pattern 2a pins with thru bottom
2 Port Differential Measurement Characterization Process

- Measure 2 port S parameters of
  - Fixture board: open, short, thru
  - Fixture + socket: open, short, thru

- Fit geophysical model terms to get agreement of simulated and measured 2 port S parameters

- Fit ideal differential pair model to geophysical model to get differential impedance

- Use model of socket (RLGC matrix values) to simulate differential insertion loss (Sdd21)

ADS Geophysical Differential Model

Fit all parameters simultaneously for open, short, thru measurement
Example of Insertion loss of Thru Measurement/Simulation

Bandwidth of the Model ~ 16 GHz

Fit Geophysical Model to Ideal, lossless diff pair model

Turn off dielectric loss in geophysical model

Z_{diff} = 68 Ohms
From Singled Ended to Differential S Parameters

\[ S_{dd11}(2,1) = 0.5 \times (S(2,1) - S(2,3) - S(4,1) + S(4,3)) \]

Differential insertion loss from 2 port measurement (based on extracted RLGC matrix values)

Conclusions

- Synergetix Characterization Method:
  - Simple, robust, reproducible
  - Non-proprietary
  - Accurate to > 10 GHz
  - Minimal and controllable artifacts
  - Output is SPICE compatible model
  - Direct measurement of model bandwidth
  - Accurate simulation of differential insertion loss

- Next step is match Agilent Momentum full wave simulation with measurement and use full wave simulation as analysis tool