Panel Discussion

“Thinner Packages And PoP Present Real Challenges For Test And Burn-in”

Moderator:
Fred Taber IBM Microelectronics (ret.)

Panelists:
Prasanth Ambady Texas Instruments IBU
Kent Carrie Amkor
Doyce Ramey Texas Instruments S/C
Jec Sangalang Yamaichi Electronics, USA

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Panel Discussion
Sunday 3/12/06 9:00PM

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Workshop Guide

Panel Discussion
Kachina Ballroom

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Effects of Stress and Temperature on Packages

• Fine pitch, bumped and LGA packaging formats drive vertical compression style sockets for burn-in.
• High pin count results in high clamping forces.

Package
Solder balls
PCB

Warp and die damage

Cracks on die, substrate and molding

• Understanding of stress, stain and thermal creep mechanisms for packages/dies.
• Defining acceptable limits of stress and deflection.
• Need for robust, open top, ZIF automated solutions.
Analysis and Techniques for Controlling Stress and Deformation

Reduced max. out of plane package deflection from 59 to 22 microns by increasing clamping surface area by 40%.

Supporting locations

Reduced max. out of plane package deflection from 85 to 32 microns and stress by 24% by moving support location.

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Technical Program

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