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Technical Program

Session 3
Tuesday 3/05/02 8:00AM

Thermal Management Methods

“Thermal Modeling Of Burn-in System”
Liu Baomin - Advanced Micro Devices

“Burn-in System And Driver Board Technology Advances”
Mike Niederhofer - - Incal Technology, Inc.
Bruce Simikowski - Incal Technology, Inc.
Liu Baomin
Senior Engineer, Advanced Micro Devices
Email: bao-min.liu@amd.com
Agenda

• Background
• Objective
• Brief Introduction of CFD Thermal Simulation
• Road Map of BI system level simulation
• Model Development & Validation
• Prediction of a new design
• Hotspot and Solution
• Conclusions
• Acknowledgement
Background

BI System Features:

• To Handle Device at high power levels.
• Active thermal control of DUT temperature.
• Forced air flow to move heat out of rack.
• PSU is placed outside main rack.

Thermal Issues to be concerned:

• Large Heat Load: around 1 KW/tray.
• Passive thermal control of critical cables & components.
• New devices
Objectives

With the prediction of the thermal and air flow profiles in the BI system, the present CFD thermal simulation is to

• Verify the thermal performance of new BI system design

• Parametric studies on device power, rack flow, ambient temperature etc.

• Predict hot spots and develop the thermal solution

• Assist to develop new innovative BI systems.
Review of CFD

• Computational Fluid Dynamics, also handle heat transfer

• Solve the governing equation sets of fluid flow & heat transfer

• Input parameters: Geometry, material properties, heat sources and flow sources (fan, pumps, etc), boundary conditions.

• Output: Velocity & temperature field

• Commercial Software for electronic system: Flotherm, Icepak, Paksi, etc.

• Flotherm V3.2 has been used in the present work.
Road Map

Project initiation
Phase 1

Information Collection

Development of Package Compact Model

Tray level model

Tray Level Measurement

Validation of Tray level model

Phase 2

Compact model development of Validated tray model

System Level Measurement

Development of Rack Model

Development of compact model for PSU

Model validation

Phase 3

Modeling of new BI System

Parametric Studies
Detail & Compact Modeling of A CPGA Package

Compact model is accepted!

<table>
<thead>
<tr>
<th>Power dissipation</th>
<th>Theta JB in detailed model °C/W</th>
<th>Theta JB in Compact model °C/W</th>
<th>% difference w.r.t detailed model</th>
</tr>
</thead>
<tbody>
<tr>
<td>10 watts</td>
<td>5.38</td>
<td>5.43</td>
<td>0.9%</td>
</tr>
<tr>
<td>40 Watts</td>
<td>5.6</td>
<td>5.48</td>
<td>2%</td>
</tr>
</tbody>
</table>
Compact Modeling of HBI Tray

• To control mesh number in each tray for system model.
• Represent detail model in air flow & temperature through tray.
• Processor, heat sink and fan assembly are lumped together.

Lumped DUT Bank
Exhaust fan, baffle, 7 compact model of trays, power supply unit (PSU),
Power supply exhaust fan, power sequence, PC, cable extenders
Tray Level Validation

- **Power measurement** of TEC, DUT, Fans, & PCB.
- **Air Temperature measurement** at 10 locations.

### Power Supply

<table>
<thead>
<tr>
<th>Position</th>
<th>Simulation Results with inlet air temperature = 25°C</th>
<th>Extrapolated results for inlet air temperature = 20.8°C</th>
<th>Measured air temperature with inlet air temperature = 20.8°C</th>
<th>% deviation w.r.t measured air temperature</th>
</tr>
</thead>
<tbody>
<tr>
<td>P1</td>
<td>38.2</td>
<td>34</td>
<td>29</td>
<td>17.2%</td>
</tr>
<tr>
<td>P2</td>
<td>45.2</td>
<td>41</td>
<td>32.4</td>
<td>26.5%</td>
</tr>
<tr>
<td>P3</td>
<td>42.1</td>
<td>37.9</td>
<td>31.7</td>
<td>19.5%</td>
</tr>
<tr>
<td>P4</td>
<td>38.3</td>
<td>34.1</td>
<td>32</td>
<td>6.5%</td>
</tr>
<tr>
<td>P5</td>
<td>42.4</td>
<td>38.2</td>
<td>33.4</td>
<td>14.3%</td>
</tr>
<tr>
<td>P6</td>
<td>37</td>
<td>32.8</td>
<td>32.3</td>
<td>1.5%</td>
</tr>
<tr>
<td>P7</td>
<td>30.9</td>
<td>26.7</td>
<td>27.4</td>
<td>2.5%</td>
</tr>
<tr>
<td>P8</td>
<td>28.9</td>
<td>24.7</td>
<td>28.3</td>
<td>12.7%</td>
</tr>
<tr>
<td>P9</td>
<td>29.1</td>
<td>24.9</td>
<td>27.4</td>
<td>9.1%</td>
</tr>
<tr>
<td>P10</td>
<td>29.6</td>
<td>25.4</td>
<td>27.3</td>
<td>6.9%</td>
</tr>
</tbody>
</table>

At most positions, the deviation is less than 15%.

Tray model is accepted.
Rack Level Validation with CPGA Package

- **Power rates** into rack, 7 PSU, PC, and 7 trays
- **Air temperature** at 20 critical locations.
- **Measured 7 times** under different conditions

<table>
<thead>
<tr>
<th>Locations</th>
<th>Thermal Couples</th>
<th>Measurement, °C</th>
<th>Simulation, °C</th>
<th>Difference, %</th>
</tr>
</thead>
<tbody>
<tr>
<td>Air guide Left</td>
<td>TC1, TC2</td>
<td>26.9</td>
<td>27.1</td>
<td>0.7</td>
</tr>
<tr>
<td>Air guide Right</td>
<td>TC3, TC4</td>
<td>27.5</td>
<td>27.1</td>
<td>-1.5</td>
</tr>
<tr>
<td>Above sequencer</td>
<td>TC5</td>
<td>25.3</td>
<td>24.2</td>
<td>-4.3</td>
</tr>
<tr>
<td>Below baffle</td>
<td>TC6</td>
<td>27.6</td>
<td>27.8</td>
<td>0.7</td>
</tr>
<tr>
<td>Tray 7 Exit</td>
<td>TC7</td>
<td>26.4</td>
<td>24.8</td>
<td>-6.1</td>
</tr>
<tr>
<td>Tray 4 Exit</td>
<td>TC8</td>
<td>28.6</td>
<td>27.0</td>
<td>-5.6</td>
</tr>
<tr>
<td>Tray 1 Exit</td>
<td>TC9</td>
<td>26.4</td>
<td>27.6</td>
<td>4.5</td>
</tr>
<tr>
<td>Tray 1 inlet</td>
<td>TC10</td>
<td>22.1</td>
<td>-</td>
<td>Ambient Temp</td>
</tr>
<tr>
<td>Tray 3 inlet</td>
<td>TC11</td>
<td>21.8</td>
<td>-</td>
<td>Ambient Temp</td>
</tr>
<tr>
<td>Tray 6 inlet</td>
<td>TC12</td>
<td>22.1</td>
<td>-</td>
<td>Ambient Temp</td>
</tr>
<tr>
<td>Tray 1 Temp</td>
<td>TC13</td>
<td>27.9</td>
<td>26.9</td>
<td>-3.6</td>
</tr>
<tr>
<td>Tray 2 Temp</td>
<td>TC14</td>
<td>28.7</td>
<td>27.9</td>
<td>-2.8</td>
</tr>
<tr>
<td>Tray 3 Temp</td>
<td>TC15</td>
<td>28.4</td>
<td>28.0</td>
<td>-1.4</td>
</tr>
<tr>
<td>Tray 4 Temp</td>
<td>TC16</td>
<td>25.6</td>
<td>28.6</td>
<td>11.7</td>
</tr>
<tr>
<td>Tray 5 Temp</td>
<td>TC17</td>
<td>28.7</td>
<td>29.3</td>
<td>2.1</td>
</tr>
<tr>
<td>Tray 6 Temp</td>
<td>TC18</td>
<td>28.2</td>
<td>28.6</td>
<td>1.4</td>
</tr>
<tr>
<td>Tray 7 Temp</td>
<td>TC19</td>
<td>22.9</td>
<td>23.6</td>
<td>3.1</td>
</tr>
<tr>
<td>Rack side</td>
<td>TC20</td>
<td>22.7</td>
<td>-</td>
<td>Ambient Temp</td>
</tr>
</tbody>
</table>

At all positions, the deviation is less than 12%.
Rack Level Validation by Electric Heaters

**Condition**
- Ambient Temperature – 30 Deg C
- Exhaust Fan Speed - 1300cfm
- Thermal Load per tray – 1200 watts
- Number of Trays per rack – 7

**Result**

<table>
<thead>
<tr>
<th>Tray Numbering</th>
<th>Measurement</th>
<th>Simulation</th>
<th>Diff %</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tray 1</td>
<td>54.3</td>
<td>51.1</td>
<td>6.24%</td>
</tr>
<tr>
<td>Tray 2</td>
<td>48.5</td>
<td>47.1</td>
<td>3.04%</td>
</tr>
<tr>
<td>Tray 3</td>
<td>45.5</td>
<td>48.1</td>
<td>-5.34%</td>
</tr>
<tr>
<td>Tray 4</td>
<td>48.0</td>
<td>49.3</td>
<td>-2.57%</td>
</tr>
<tr>
<td>Tray 5</td>
<td>43.9</td>
<td>49.6</td>
<td>-11.40%</td>
</tr>
<tr>
<td>Tray 6</td>
<td>47.3</td>
<td>51.6</td>
<td>-8.25%</td>
</tr>
<tr>
<td>Tray 7</td>
<td>46.6</td>
<td>50.5</td>
<td>-7.70%</td>
</tr>
</tbody>
</table>

Simulation agrees with measurement at difference less than 12%.

Rack level model is accepted!
Application to New BI Design: DUT Unit

Device Fan

High performance heat sink

Copper thermal plate

uP package
Modeling of New BI Tray

- PCBs: V board, F-Board, S-board & T board.
- Components: Voltage Regulator Modules (VRMs), Convert block
- 3 Tray Fans, Cable & its connector
Modeling of New BI Rack
Typical Flow & Thermal Distributions

Design conditions:

- $uP = 45W$; $TEC=30W$
- $VRM = 15.6W$
- Totally, $1.25KW/tray$, $11.65W/rack$.  
- Ambient: $25°C$
- Rack Fan: $1392$ CFM

Predictions:

<table>
<thead>
<tr>
<th>Tray Temperature, 'C:</th>
<th>Tray 1</th>
<th>Tray 2</th>
<th>Tray 3</th>
<th>Tray 4</th>
<th>Tray 5</th>
<th>Tray 6</th>
<th>Tray 7</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>48.0</td>
<td>43.6</td>
<td>43.9</td>
<td>44.3</td>
<td>44.5</td>
<td>44.6</td>
<td>44.7</td>
</tr>
</tbody>
</table>
Animation of Air Flow in BI Rack
Hot Spots in the Present Design

VRMs are at about 500°C, Hot spots in the rack!
Thermal Solution to Hot Spots by Heat Bridge

<table>
<thead>
<tr>
<th>Tray</th>
<th>VRM1</th>
<th>VRM2</th>
<th>VRM3</th>
<th>VRM4</th>
<th>VRM5</th>
</tr>
</thead>
<tbody>
<tr>
<td>Temp, 'C</td>
<td>94</td>
<td>101</td>
<td>103</td>
<td>103</td>
<td>96</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Tray Temperature, 'C:</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tray 7</td>
</tr>
<tr>
<td>43.7</td>
</tr>
</tbody>
</table>

Achievement: VRM Temp < 150°C, Tray Temp reduced by about 1°C.
Conclusions

- Thermal simulation methodology for BI system have been developed with validations.
- New BI system design have been modeled and hot spots were detected on VRMs.
- Methods has been developed to solve the thermal issues.
- CFD modeling can be used to evaluate, improve the system design, and prevent the thermal issues before manufacturing and production and thus time-saving and cost-saving.
Benefits of Thermal Simulation

- Procedures to develop and validate the CFD models for complicated systems.
- Compact model development methodology for component and sub-system.
- Validation experiment at subsystem and full system level
- Experience and knowledge can be used to simulate other testing equipment and systems.
Acknowledgement

The following persons are acknowledged for their respective contributions and support to the project:

• Bay Gim Leng, Rathin Mandal, Mui Yew Cheong, Rafiq Hussain, Maung, MS, James Hayward, Raj Master, AW CK and CS Chan from AMD.

• D.Pinjala, O.K.Navas from Institute of Microelectronics (Singapore)

Support of AMD management is also appreciated.
BiTS 2002
Burn-in System
and
Driver Board
Technology Advances

2002 Burn-in and Test Socket Workshop
March 3 - 6, 2002

Mike Niederhofer, & Bruce Simikowski
INCAL Technology, Inc.
Burn-in System
Minimum Requirements

- Temperature control
- Power supply control and sequencing
- Dynamic drive signal capabilities
- Downloadable pattern file structures
Past Burn-in system technology

- Static Burn-in
- Dynamic drivers with binary counter or EE Ori prom based drivers
- No output monitoring - manual operator measurement
- Manual power supply sequencing or thumb-wheel switches
- Temperature monitor via chart recorder
Early Burn-in systems

• The OLD way
Today’s customers demand

- Flexible system tooling for different board types
- Windows based op system - Windows NT
- Network access - Desktop Emulation
- Output monitoring
- Lower voltage levels - 0.5 volts for <.13 micron tech.
- Higher frequencies - to 33 MHz
- BIST test functions
- DUT Status, failure data analysis
- Pattern editors
- Tester vector converters
Modern Burn-in Systems

- Computerized
- Low Voltages
- DUT Monitoring
Windows Op sys

- Vertical
- or
- Horizontal
Slot Information

- DUT Mapping
- Waveform retrieval example
- Advanced fail information
Pattern Editor Program
Tester Vector conversions

- A Difficult Challenge
Previous Driver capabilities

• 16 address lines / eight clocks
• Clock outputs in ranges of 5 to 10 volts
• Maximum frequency of 2 to 10 MHz
• No on-board memory. Pattern Generators configured on a zone basis.
• 96 channels maximum
• Discrete Output channels
Latest driver board technology requirements

- Computer controlled
- Tester file Compatibility
- Configurable Drive and Monitor channels
- Speeds of > 25 MHz
- Memory pattern depth 2 to 16 Meg
- Monitor of DUT outputs
- 128 to 256 channels
- Compatible to many signal types: TTL, LVTTTL, LVDS, PECL, GTL, GTL+, CML
Modern Drivers
Dedicated driver boards

- Application specific or
- Industry specific
- Surface mount technology
- High production volumes
- Lower unit cost
Dedicated driver boards

- Application specific Drivers
  - HTRB/HTGS
  - HYBRID
  - Electro Migration
  - Soft-Error
High Power System & Driver requirements

- Designed specifically for Hi-Voltage FET, IGBT, SSR testing
- High voltage capabilities
- Individual DUT power Control/Monitoring
- Automotive market
- Industrial Controls Market
Specialty B/I system specifications

- Computer controlled
- Individual DUT monitoring
New emerging test methodologies

- Soft Error testing
- Test memory locations with neutron or proton sources present
Today’s Industry markets and requirements

<table>
<thead>
<tr>
<th>MARKET</th>
<th>REQUIREMENTS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Commercial IC market</td>
<td>Low cost / delivery</td>
</tr>
<tr>
<td>Automotive market</td>
<td>High power</td>
</tr>
<tr>
<td>Memory market</td>
<td>Speed / error detect</td>
</tr>
<tr>
<td>Medical / Military</td>
<td>Custom hardware</td>
</tr>
<tr>
<td>Test Lab market</td>
<td>Cost / flexibility</td>
</tr>
</tbody>
</table>
Today’s industry demands

- High speed dynamic drive
- High power dissipation
- Deeper pattern requirements
Specialty and Hybrid market specifications

- Implantable Devices
- High Quality levels required
- Custom Hybrids and sockets
- High Voltage Power and Signals
- Monitor capabilities required
Test Lab market

- Low cost, universal hardware
- Adapter trays to utilize existing BIBS
- Flexibility
- Ease of Pattern Generation & Conversion
System vendor’s plight

- A typical System engineering dilemma

<table>
<thead>
<tr>
<th>Sales price</th>
<th>R &amp; D costs</th>
</tr>
</thead>
</table>

Ratio
Customer’s requirements

- A perfect solution for the customer
Burn-in system vendor

• One stop shopping

Production chambers
Prescreen stations
lab ovens

Custom software
Pattern conversions

BIBS
Drivers

Customer

Service
and support
Conclusion

• Vendors and customers work towards common goal of improving technology while lowering costs
• Standardization of hardware
• Sharing of R & D costs
• Discuss technology advancements and technical requirements up-front
• Service multiple markets with present technology
• Industry consolidation inevitable
Conclusion

• Today we see Production systems that offer the flexibility to test and burn-in different product types and technologies for many different markets

• The cost of these Burn-in systems can approach those of high-end VLSI testers
Conclusion

• A working relationship between the system vendor and the customer at all stages of the purchase and utilization cycle will reduce R & D costs, thus lowering system costs.

• NRE charges, design costs, custom hardware, and custom software ... WILL ALWAYS EXIST
Conclusion

• Minimizing these costs, while providing the customer cost effective technical solutions

Is the CHALLENGE system vendors face today