Burn-in & Test Socket Workshop

March 4 - 7, 2001
Hilton Mesa Pavilion Hotel
Mesa, Arizona

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Burn-in & Test Socket Workshop

Technical Program

Keynote Speaker
Monday 3/05/01 8:00PM

“Wafer Level Paradigm For Burn-in And Test”

Dr. Thomas Di Stefano
President & CEO
Decision Track, LLC
Wafer-Level Paradigm for Burn-in and Test

Dr. Thomas Di Stefano
Decision Track
March 5, 2001
Chip Scale / Wafer Level Packaging Begins a New Paradigm

- **Surface Mount**
  - QFP
  - TSOP
  - SOJ
  - BGA

- **Chip Scale**
  - CSP
  - Wafer Level
  - Stacked Die
  - SiP

- **Thru Hole**
  - DIP
  - Pin Grid

**YEAR**

- **1960**
- **1980**
- **2000**

**VOLUME**

**Density**
**IC Packaging Progression:**

- **Through Hole**
  - DIP
    - 100 mil pitch
    - Limited by through hole spacing

- **Surface Mount**
  - TSOP
    - 25 mil pitch
    - Limited by perimeter leads

- **CSP / WLP**
  - CSP
    - Area array 0.8 mm to 0.5 mm
    - Limited by substrate wiring
Packaging Driver: Miniaturization

- Personal Electronics -
  - Cell Phones
  - PDAs
  - Camcorders
  - Mobile Computers
  - Card PCs
  - Memory Cards
  - Personal Communicators
Wafer Level Packaging and Interconnect... Enabled by the Chip Size Package

• The Wafer Level Paradigm is driven by imperatives ...
  – Packaging Cost
  – Simplified Logistics
  – IC Functionality
  – Performance

• Production is Emerging Rapidly
  – Beginning in Small Devices (< 3mm)
  – Adapts Wafer Processing Infrastructure
  – Extending to Larger Die Sizes
Dallas Semiconductor Wafer Level Package
National Semiconductor MicroSMD
Wafer Level Packaging is Paced by Infrastructure

- Package Reliability
- High Density PWB Substrates
- Burn-in and Test
  - Wafer level burn-in
  - Functional test on the wafer
- Standards
  - Proliferation of variations slows adoption
Flip-Chip Wafer Level Package

• Eutectic Solder Ball Flip-Chip
  – Small DNP allows adequate reliability
  – Adapts existing infrastructure for rapid growth
    ... But --- limited to small die sizes

• Flexible Interconnect Extends to Larger Die Sizes
  – Metal columns
  – Solder columns
  – Stacked solder balls
  – Flexible solder balls
    ... All with minimum changes to existing wafer processing infrastructure

• Wafer Level Package Provides:
  – Surface mountable package
  – Testability
  – Reliability
  – Standards
Fujitsu SuperCSP

- Solder balls on copper posts
- Redistribution wiring to posts
- Encapsulant is molded onto wafer
- Inflexible posts limit reliability
APACK Solder Column Package

Improves Strain Relief on Solder Ball
<table>
<thead>
<tr>
<th>Pins (#)</th>
<th>Die Area (mm²)</th>
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<tr>
<td>1</td>
<td>1</td>
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<tr>
<td>10</td>
<td>10</td>
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<td>100</td>
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<tr>
<td>1000</td>
<td>1000</td>
</tr>
<tr>
<td>10000</td>
<td>10000</td>
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</table>

- **Flip-Chip**
- **Underfill+**
- **µProcessor**
- **0.25 mm grid**
- **0.5 mm grid**
- **HDI PW**
- **ASICS**
- **DRAM**
- **SRAM**
- **Passives**
- **Analog ICs**
- **Power ICs**
- **Discretes**

Flexible Contacts Will Extend Wafer Level (2002-2005)
JIEP Projections for CTE


CTE (ppm/C):
- Board
- Package

Graph showing trends for Board and Package CTE from 1998 to 2010.
Low CTE Substrates Further Extend Wafer Level (2005)
CSPWLP Paced by High Density Substrate

- CSP
- Stacked Die
- WLP
- SiP
- μPROCESSOR
- WIRELESS
- ASICS
- INFORMATION APPLIANCES
- FLASH, SRAM
- DSP
- DRAM

Requires HDI

1995 2000 2005 2010

Decision Track BiTS 2001
### World Micro-via Hole PCB Production ($million)

<table>
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<tr>
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<tr>
<td>Japan</td>
<td>320</td>
<td>600</td>
<td>1,055</td>
<td>1,800</td>
<td>2,700</td>
<td>4,000</td>
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<tr>
<td>Europe</td>
<td>10</td>
<td>15</td>
<td>40</td>
<td>260</td>
<td>400</td>
<td>600</td>
</tr>
<tr>
<td>N. America</td>
<td>25</td>
<td>35</td>
<td>40</td>
<td>150</td>
<td>300</td>
<td>500</td>
</tr>
<tr>
<td>Asia Pacific</td>
<td>2</td>
<td>10</td>
<td>85</td>
<td>210</td>
<td>400</td>
<td>600</td>
</tr>
<tr>
<td><strong>Total</strong></td>
<td>357</td>
<td>660</td>
<td>1,220</td>
<td>2,420</td>
<td>3,800</td>
<td>5,700</td>
</tr>
</tbody>
</table>

**Total Number of Lasers**

|                  | 115  | 240  | 450  | 900  | 1,500 | 2,500 |

*forecast - Japan’s $4 Billion 2001 forecast consists of $2.5 Billion IC package (BGA/LGA) substrates and $1.5 Billion in HDI circuit boards.*

Data Source: N.T. Information Ltd. (Dr. Hayao Nakahara)
**I/O Explosion: Power & Ground Distribution**

- **Distribute the Power and Ground on Chip**
  - Better electrical characteristics
  - Shorter distance to the shielding planes
  - Dramatically reduces I/O connections for power/ground
    - 80+% of I/O on advanced processors is Power/Ground.

- **Power and Ground Layers on the Wafer**
  - Efficiency of production
    - Avoid paying for large number of power/ground pins.
  - Makes the chip easier to test - fewer power/ground contacts
The graph shows the growth of interconnect-related parameters over time. The time line is divided into three decades: 1980, 1990, and 2000.

- **I/O (Input/Output)**: This parameter has shown a steady increase, with a significant rise towards 2000.
- **Power/Ground**: The power and ground lines are also on an upward trend, particularly noticeable by the year 2000.
- **Total Pin Count**: This parameter experiences a dramatic increase, especially from 1990 onwards, reaching a high by 2000.

The graph illustrates the explosive growth in interconnect requirements, which has significant implications for the design and development of modern electronic systems.
IC Performance: RC Delays are an Increasing Problem

RC Delays scale as the inverse square of the scaling law
- Max propagation length is 3 mm at 0.25 μm lithography
- Propagation length shrinks as geometries are scaled
**Power & Ground: Redistribution on the Chip**

**Power/Ground Distribution**
- Fabricated on separate layers
- Assembled to the wafer

**Flip Chip**
- Pin count Explosion
- 70-80% is Power & Ground

**Composite Chip**
- Power/ground distributed on the chip to reduce I/O count
- High performance Power and ground distribution
Wafer Level Packaging: Added Interconnect Capability

- Wafer level production for processors allows
  - Power/ground distribution on chip
  - Routing critical nets in low resistance copper lines in the package

- Approaches
  - Multi-layer flex interposer
  - Silicon interposer

- Pacing items
  - High density wiring capability on chip for (4-6 layers of wiring)
  - High density PWB substrates (0.5 mm via pitch or better)
  - Capability to burn-in and test chips in a wafer format
**Multi-Chip Packages: MCMs?**

**Multi-Chip Packages Offer MCM Advantages**

- Avoid Large Die Sizes of System-on-a-Chip
- Faster Time-to-Market
- Mixed Technologies (GaAs, Flash, Passives, …)
- Smaller Size
- Higher Performance

**So What’s New?**

- Wafer Test and Burn-in of Wafer Level Packages
- High Volume Applications
- Cost Effective Micro-via Substrates
SyChip Integrated Phone-in-a-Package Solution
Wafer Test & Burn-in: Driving Factors

- **Necessary for Wafer Level Packaging**
  - Must burn-in Before Final Test on the Wafer.
  - Applies to flip chip as well as full wafer level packaging

- **Faster Time to Market**
  - Diced Wafer is the final, fully tested product.

- **Faster Cycles of Learning**
  - The wafer fab has full information on test before wafer leaves fab

- **Reduction of Test Costs**
  - “Test Once”
  - Wafer test is both probe and final test
**Conventional Packaging**

- Wafer Probe
- Wafer Dicing
- Package
- Test
- Burn-in
- Final Test

**Wafer Level Packaging**

- Wafer Packaging
- Wafer Burn-in
- Final Test
- Wafer Dicing

- Product Cost Reduction
- Cycle Time Reduction
- Capital Cost Reduction
Wafer Test: Challenges Ahead

- **Probe Density**
  - 60 μm pad spacing
  - Area array pads

- **Functional Wafer Test**
  - Test at Speed

- **Parallel Testing**
  - BIST ?
  - Wafer run-in (test during burn-in)

- **Hot chuck testing**
  - Wafer test at temperatures to 150 °C
**Wafer Burn-in: Technical Challenges**

- **Contact Alignment**
- **Electrical Interconnect**
  - Wire 10,000 - 20,000 contacts to device drivers
- **Large Number of Electrical Contacts**
  - Force of 250 lb for 20,000 contacts
  - 500,000 contacts for a flip chip micro-Processor
- **Extreme Environment**
Wafer **Burn-in**: Technical Challenges

- 10,000 - 500,000 contacts

- From 25°C to 150°C
  - Cu → 450 µm (18 mils)
  - Si → 75 µm (3 mils)
The Drive Toward Wafer Level Packaging

• Growth of Chip Scale Electronics is Rapid

• Chip Scale is Moving toward Wafer Level Packaging

• Wafer Level Packaging will Extend for Decades into the Future

• Advances are Needed in Burn-in and Test
  - Strip Test
  - Wafer Test at Speed
  - Wafer Level Burn-In